7 SYSTEM INTERFACE

Overview

This chapter describes the basic system interface features of the ADSP-218x family processors. The system interface includes various hardware and software features used to control the DSP processor.

Processor control pins include a $\overline{\text{RESET}}$ signal, clock signals, flag inputs and outputs, and interrupt requests. This chapter describes only the logical relationships of control signals; consult individual processor data sheets for actual timing specifications.

Pin Descriptions

This section provides functional descriptions of the ADSP-218x processor pins. Because processors come in different packages, there are some differences in the pins contained on each. Table 7-1 shows the package configurations for each ADSP-218x processor and the sections that follow identify the pins for each package.

Table 7-1. ADSP-218x Processor Package Configurations

Processor	Package
ADSP-2181	128-LQFP and 128-MQFP
ADSP-2183	128-LQFP and 144-Mini-BGA

Table 7-1. ADSP-218x Processor Package Configurations (Cont'd)

Processor	Package
ADSP-2184	100-LQFP
ADSP-2184L[1]	100-LQFP
ADSP-2184N[3]	100-LQFP and 144-miniBGA
ADSP-2185	100-LQFP
ADSP-2185L[1]	100-Lead LQFP and 144-Mini-BGA
ADSP-2185M[2]	100-LQFP and 144-miniBGA
ADSP-2185N[3]	100-LQFP and 144-miniBGA
ADSP-2186	100-LQFP and 144-Mini-BGA
ADSP-2186L[1]	100-LQFP and 144-Mini-BGA
ADSP-2186M[2]	100-LQFP and 144-Mini-BGA
ADSP-2186N[3]	100-LQFP and 144-miniBGA
ADSP-2187L[1]	100-LQFP
ADSP-2187N[3]	100-LQFP and 144-miniBGA
ADSP-2188M[2]	100-LQFP and 144-Mini-BGA
ADSP-2188N[3]	100-LQFP and 144-miniBGA

Table 7-1. ADSP-218x Processor Package Configurations (Cont'd)

Processor	Package
ADSP-2189M[2]	100-LQFP and 144-Mini-BGA
ADSP-2189N[3]	100-LQFP and 144-miniBGA

1 L indicates that the processor operates at 3.3 V. These processors are not tolerant to 5 V inputs

2 M indicates that the processor core operates at 2.5 V and that the external I/O can operate between 2.5 V and 3.3 V. The external I/O is tolerant to up to 3.6 V inputs with a supply voltage between 2.5 V and 3.3 V. However, it is not tolerant to 5 V inputs.

3 N indicates that the processor core operates at11.8 V and that the external I/O can operate between 1.8 V or 3.3 V. The external I/O is tolerant to up to 3.6 V inputs with a supply voltage of 1.8 V or 3.3 V. However, it is not tolerant to 5 V inputs.

Pin Descriptions for 128-LQFP Package Processors

Unlike the other ADSP-218x processors, the ADSP-2181 and ADSP-2183 processors come in 128-LQFP and 128-MQFP packages. For these two processors, the full address, data, and IDMA port signals are brought out to external pins. The remainder of the ADSP-218x processors, which come in 100-LQFP packages, multiplex the address bus and a portion of the data bus to achieve a lower package pinout.

Table 7-2 provides a description of the ADSP-2181 and ADSP-2183 processor pins. All pin descriptions also apply to the ADSP-2183 processor in the 144-Lead Mini-BGA package unless otherwise noted.

Table 7-2. ADSP-2181 and ADSP-2183 Processor Pin Descriptions

Pin Name(s)	# of Pins	I/O	Function
Address	14	O	Address Output Pins for Program, Data, Byte, and I/O spaces
Data	24	I/O	Data I/O Pins for Program and Data Memory Spaces (8 MSBs are also used as Byte Space Addresses
$\overline{\text{RESET}}$	1	I	Processor Reset Input
$\overline{\text{IRQ2}}$	1	I	Edge- or Level-Sensitive Interrupt Request
$\overline{\text{IRQL0}}$ $\overline{\text{IRQL1}}$	1 1	I I	Level-Sensitive Interrupt Requests
$\overline{\text{IRQE}}$	1	I	Edge-Sensitive Interrupt Requests
$\overline{\text{BR}}$	1	I	Bus Request Input
$\overline{\text{BG}}$	1	O	Bus Grant Output
$\overline{\text{BGH}}$	1	O	Bus Grant Hung Output
$\overline{\text{PMS}}$	1	O	Program Memory Select Output
$\overline{\text{DMS}}$	1	O	Data Memory Select Output
$\overline{\text{BMS}}$	1	O	Byte Memory Select Output
$\overline{\text{IOMS}}$	1	O	Memory Select Output

Table 7-2. ADSP-2181 and ADSP-2183 Processor Pin Descriptions (Cont'd)

Pin Name(s)	# of Pins	I/O	Function
$\overline{\text{CMS}}$	1	O	Combined Memory Select Output
$\overline{\text{RD}}$	1	O	Memory Read Enable Output
$\overline{\text{WR}}$	1	O	Memory Write Enable Output
MMAP	1	I	Memory Map Select Input
BMODE	1	I	Boot Option Control Input
CLKIN XTAL	2	I	Clock or Quartz Crystal Input
CLKOUT	1	O	Processor Clock Output
SPORT0	5	I/O	Serial Port I/O Pins
SPORT1	5	I/O	Serial Port1 or two external $\overline{\text{IRQ}}$s, Flag In and Flag Out
$\overline{\text{IRD}}$ $\overline{\text{IWR}}$	2	I	IDMA Port Read/ Write Inputs
$\overline{\text{IS}}$	1	I	IDMA Port Select
IAL	1	I	IDMA Port Address Latch Enable
IAD	16	I/O	IDMA Port Address/Data Bus
$\overline{\text{IACK}}$	I	O	IDMA Port Access Ready
$\overline{\text{PWD}}$	1	I	Powerdown Control Input
PWDACK	I	O	Powerdown Control Output

Table 7-2. ADSP-2181 and ADSP-2183 Processor Pin Descriptions (Cont'd)

Pin Name(s)	# of Pins	I/O	Function
FL0, FL1, FL2	3	O	Output Flags
PF7:0	8	I/O	Programmable I/O Pins
EE	1	*	Emulator only*
$\overline{\text{EBR}}$	1	*	Emulator only*
$\overline{\text{EBG}}$	1	*	Emulator only*
$\overline{\text{ERESET}}$	1	*	Emulator only*
$\overline{\text{EMS}}$	1	*	Emulator only*
$\overline{\text{EINT}}$	1	*	Emulator only*
ECLK	1	*	Emulator only*
ELIN	1	*	Emulator only*
ELOUT	1	*	Emulator only*

Table 7-2. ADSP-2181 and ADSP-2183 Processor Pin Descriptions (Cont'd)

Pin Name(s)	# of Pins	I/O	Function
V_{DD}	6		Power
GND	11		Ground
(Applies to ADSP-2181 and ADSP-2183 in 128-LQFP package only)			
V_{DD}	11		Power
GND	22		Ground
(Applies to ADSP-2183 in 144-Lead Mini-BGA package only)			

* These pins must be connected only to the EZ-ICE connector in the target system. These pins have no function except during emulation and do not require pull-up or pull-down resistors.

Pin Descriptions for 100-LQFP Package Processors

In order to maintain maximum functionality and reduce package size and pin count in the 100-LQFP packages, some serial port, programmable flag, interrupt, and external bus pins have dual, multiplexed functionality. The external bus pins are configured during $\overline{\text{RESET}}$ only, while serial port pins are software configurable during program execution.

The programmable flag pins on the ADSP-218x 100-LQFP processors retain the same functionality as those on the ADSP-2181 and ADSP-2183 128-LQFP packages but share these pins with interrupt pins. The programmable flag pins PF[7:4] are shared with interrupts $\overline{\text{IRQ2}}$, $\overline{\text{IRQL1}}$, $\overline{\text{IRQL0}}$, and $\overline{\text{IRQE}}$, respectively. Both the programmable flags and interrupts are directly connected to the shared pins. You use existing control registers to choose the desired function for each pin. Each pin has four possible states:

- IMASK[x]=0, PFTYPE[x]=0(PF Input)
    - Read of PFDATA gives pin value
    - No interrupt occurs
    - Default after reset
- IMASK[x]=1, PFTYPE[x]=0(PF Input)
    - Read of PFDATA gives pin value
    - Interrupt occurs on level- or edge-transition
- IMASK[x]=0, PFTYPE[x]=1(PF Output)
    - Write to PFDATA sets pin value
    - Read of PFDATA gives set value
    - No interrupt occurs
- IMASK[x]=1, PFTYPE[x]=1(PF Output)
    - Write to PFDATA sets pin value and may cause interrupt (level- or edge-sensitive)
    - Read of PFDATA gives set value

After reset, the PF pins default to inputs and the interrupts are disabled by the IMASK register's default value. The pins can be used as PF outputs by changing the PFTYPE register and leaving the interrupt disabled in IMASK. If the pins are to be used as interrupts, then the PFTYPE register need not be changed, but the interrupt must be enabled in the IMASK register.

Common-Mode Pins

Table 7-3 provides a description of the pins that are common to both Full Memory Mode and Host Memory Mode in 100-LQFP packages. In cases where pin functionality is reconfigurable, the default state is shown in plain text; alternate functionality is shown in *italics*. All pin descriptions also apply to the processors in 144-Ball Mini-BGA packages unless otherwise noted.

Table 7-3. Common-Mode Pins

Pin Name(s)	Number of Pins	I/O	Function
$\overline{\text{RESET}}$	1	I	Processor Reset Input
$\overline{\text{BR}}$	1	I	Bus Request Input
$\overline{\text{BG}}$	1	O	Bus Grant Output
$\overline{\text{BGH}}$	1	O	Bus Grant Hung Output
$\overline{\text{DMS}}$	1	O	Data Memory Select Output
$\overline{\text{PMS}}$	1	O	Program Memory Select Output
$\overline{\text{IOMS}}$	1	O	Memory Select Output
$\overline{\text{BMS}}$	1	O	Byte Memory Select Output
$\overline{\text{CMS}}$	1	O	Combined Memory Select Output

Table 7-3. Common-Mode Pins (Cont'd)

Pin Name(s)	Number of Pins	I/O	Function
$\overline{\text{RD}}$	1	O	Memory Read Enable Output
$\overline{\text{WR}}$	1	O	Memory Write Enable Output
$\overline{\text{IRQ2}}$ *PF7*	1	I I/O	Edge- or Level-Sensitive Interrupt Request[1] Programmable I/O Pin
$\overline{\text{IRQL1}}$ *PF6*	1	I I/O	Level-Sensitive Interrupt Requests[1] Programmable I/O Pin
$\overline{\text{IRQL0}}$ *PF5*	1	I I/O	Level-Sensitive Interrupt Requests[1] Programmable I/O Pin
$\overline{\text{IRQE}}$ *PF4*	1	I I/O	Edge-Sensitive Interrupt Requests[1] Programmable I/O Pin
Mode D *PF3*	1	I I/O	Mode Select Input - Checked only during $\overline{\text{RESET}}$ Programmable I/O Pin during normal operation
Mode C *PF2*	1	I I/O	Mode Select Input - Checked only during $\overline{\text{RESET}}$ Programmable I/O Pin during normal operation
Mode B *PF1*	1	I I/O	Mode Select Input - Checked only during $\overline{\text{RESET}}$ Programmable I/O Pin during normal operation
Mode A *PF0*	1	I I/O	Mode Select Input - Checked only during $\overline{\text{RESET}}$ Programmable I/O Pin during normal operation
CLKIN XTAL	2	I	Clock or Quartz Crystal Input

Table 7-3. Common-Mode Pins (Cont'd)

Pin Name(s)	Number of Pins	I/O	Function
CLKOUT	1	O	Processor Clock Output
SPORT0	5	I/O	Serial Port I/O Pins
SPORT1 $\overline{\text{IRQ1:0}}$, FI, FO	5	I/O	Serial Port I/O Pins Edge- or Level-Sensitive Interrupts, Flag In, Flag Out[2]
$\overline{\text{PWD}}$ PWDACK FL0, FL1, FL2	1 I 3	I O O	Powerdown Control Input Powerdown Control Output Output Flags
V_{DD} GND	6 10	I I	Power Ground
(Applies to all ADSP-2184, ADSP-2184L, ADSP-2185, ADSP-2185L, ADSP-2186, ADSP-2186L, ADSP-2187L processors in 100-Lead LQFP package only)			
V_{DD} GND	11 20	I I	Power Ground
(Applies to ADSP- 2185L, ADSP-2186, and ADSP- 2186L processors in 144-Mini-BGA package only)			
V_{DDINT} V_{DDEXT} GND	2 4 10	I I I	Internal V_{DD} (2.5V) Power External V_{DD} (2.5V or 3.3V) Power Ground
(Applies to all ADSP-218x M and N series processors in 100-Lead LQFP package only)			

Table 7-3. Common-Mode Pins (Cont'd)

Pin Name(s)	Number of Pins	I/O	Function
V_{DDINT}	4	I	Internal V_{DD} (2.5V) Power
V_{DDEXT}	7	I	External VDD (2.5V or 3.3V) Power
GND	20	I	Ground
(Applies to all ADSP-218x M and N series processors in 144-Ball Mini-BGA package only)			
EZ-Port	9	I/O	For emulation use

1 Interrupt/Flag Pins retain both functions concurrently. If IMASK is set to enable the corresponding interrupts, then the DSP will vector to the appropriate interrupt vector address when the pin is asserted, either by external devices, or set as a programmable flag.
2 SPORT configuration determined by the DSP System Control register. Software configurable.

Memory Mode Pins

Table 7-4 provides a description of Full Memory Mode pins and Table 7-5 provides a description of the Host Memory Mode pins on ADSP-218x processors in 100-lead LQFP and 144-MBGA packages.

Table 7-4. Full Memory Mode Pins (Mode C = 0)

Pin Name	Number of Pins	I/O	Function
A13:0	14	O	Address Output Pins for Program, Data, Byte and I/O Spaces
D23:0	24	I/O	Data I/O Pins for Program, Data, Byte and I/O Spaces (8 MSBs are also used as Byte Memory addresses)

Table 7-5. Host Memory Mode Pins (Mode C = 1)

Pin Name	Number of Pins	I/O	Function
IAD15:0	16	I/O	IDMA Port Address/Data Bus
A0	1	O	Address Pin for External I/O, Program, Data, or Byte access[1]
D23:8	16	I/O	Data I/O Pins for Program, Data Byte and I/O spaces
$\overline{\text{IWR}}$	1	I	IDMA Write Enable
$\overline{\text{IRD}}$	1	I	IDMA Read Enable
IAL	1	I	IDMA Address Latch Pin
$\overline{\text{IS}}$	1	I	IDMA Select
$\overline{\text{IACK}}$	1	O	IDMA Port Acknowledge Configurable in Mode D; Open Drain

1 In Host Mode, external peripheral addresses can be decoded using the A0, $\overline{\text{CMS}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, and $\overline{\text{IOMS}}$ signals.

Active or Passive Mode Pin Configuration

To decrease the package size of the ADSP-218x family processors for the 100-LQFP packages, the IDMA bus and associated control signals are multiplexed with the external Address and Data busses. The logic value of the Mode pins are latched on the rising edge of the $\overline{\text{RESET}}$ signal. The values of the Mode pins determine whether the DSP will boot from an EPROM or be booted from an external host processor.

The Mode pins also determine whether the DSP's external pins are used for IDMA accesses (Host Memory mode) or whether the full 14-bit address bus and 24-bit data bus is active (Full Memory mode).

The Mode pins can be set for active or passive configuration. An active configuration means that the Mode pin is used as a Mode pin during reset, but also functions alternately as a Programmable Flag pin or Interrupt Signal during runtime. Passive configuration means that the Mode pin is used only as a Mode pin and has no alternate function during runtime.

A passive configuration is more easily implemented because only a simple pullup or pulldown resistor is needed to maintain a proper logic level for the Mode pin. (Tying a Mode pin directly to V_{DD} or GND is also acceptable.)

An Active configuration requires either a weak pullup or pulldown (on the order of 100 kΩ) or some type of tristate driver or logic gate to allow for proper operation of the pin during its alternate mode of functioning as a Programmable Flag pin or Interrupt signal. (A weak pullup or pulldown resistor is used to reduce the amount of current flow to the input pin of the DSP and to minimize the amount of current going through an output driver.) For more information on setting the Mode pins for an active or passive configuration, please see "Using Mode Pins with RESET and ERESET Signals" on page 7-64.

Terminating Unused Pins

Table 7-6 shows the recommendations for terminating unused pins. Additional recommendations follow the table.

Table 7-6 shows the multiplexed pins for the Host Memory mode and Full Memory mode of the 100-pin processors. These multiplexed pins are grouped in pairs. The pins listed in this table also apply to the ADSP-2181 and ADSP-2183 processors.

Table 7-6. Pin Terminations

Pin Name	I/O Tri-State (Z)	Reset State	Hi-Z* Caused By…	Unused Configuration
XTAL	I	I		Float
CLKOUT	O	O		Float
A13:1 or IAD 12:0	O (Z) I/O (Z)	Hi-Z Hi-Z	$\overline{BR}$, $\overline{EBR}$ $\overline{IS}$	Float Float
A0	O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
D23:8	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
D7 or $\overline{IWR}$	I/O (Z) I	Hi-Z I	$\overline{BR}$, $\overline{EBR}$	Float High (Inactive)
D6 or $\overline{IRD}$	I/O (Z) I	Hi-Z I	$\overline{BR}$, $\overline{EBR}$	Float High (Inactive)
D5 or IAL	I/O (Z) I	Hi-Z I		Float Low (Inactive)
D4 or $\overline{IS}$	I/O (Z) I	Hi-Z I	$\overline{BR}$, $\overline{EBR}$	Float High (Inactive)
D3 or $\overline{IACK}$	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float Float
D2:0 or IAD15:13	I/O (Z) I/O (Z)	Hi-Z Hi-Z	$\overline{BR}$, $\overline{EBR}$ $\overline{IS}$	Float Float
$\overline{PMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{DMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{BMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float

Table 7-6. Pin Terminations (Cont'd)

Pin Name	I/O Tri-State (Z)	Reset State	Hi-Z* Caused By…	Unused Configuration
$\overline{\text{IOMS}}$	O (Z)	O	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float
$\overline{\text{CMS}}$	O (Z)	O	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float
$\overline{\text{RD}}$	O (Z)	O	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float
$\overline{\text{WR}}$	O (Z)	O	$\overline{\text{BR}}$, $\overline{\text{EBR}}$	Float
$\overline{\text{BR}}$	I	I		High (Inactive)
$\overline{\text{BG}}$	O (Z)	O	EE	Float
$\overline{\text{BGH}}$	O	O		Float
$\overline{\text{IRQ2}}$/PF7	I/O (Z)	I		Input = High (Inactive) or program as Output, Set to 1, Let float
$\overline{\text{IRQL1}}$/PF6	I/O (Z)	I		Input = High (Inactive) or program as Output, Set to 1, Let float
$\overline{\text{IRQL0}}$/PF5	I/O (Z)	I		Input = High (Inactive) or program as Output, Set to 1, Let float
$\overline{\text{IRQE}}$/PF4	I/O (Z)	I		Input = High (Inactive) or program as Output, Set to 1, Let float
SCLK0	I/O	I		Input = High or Low, Output = Float

Table 7-6. Pin Terminations (Cont'd)

Pin Name	I/O Tri-State (Z)	Reset State	Hi-Z* Caused By…	Unused Configuration
RFS0	I/O	I		High or Low, Let float if SPORT0 is disabled
DR0	I	I		High or Low, Let float if SPORT0 is disabled
TFS0	I/O	I		High or Low, Let float if SPORT0 is disabled
DT0	O	O		Float
SCLK1	I/O	I		Input = High or Low, Output = Float
RFS1/$\overline{\text{IRQ0}}$	I/O	I		High or Low
DR1/FI	I	I		High or Low, Float if SPORT1 is disabled and the pin is not configured as FI
TFS1/$\overline{\text{IRQ1}}$	O/I	I		High or Low
DT1/FO	O	O		Float
EE	I	I		Float
$\overline{\text{EBR}}$	I	I		Float
$\overline{\text{EBG}}$	O	O		Float
$\overline{\text{ERESET}}$	I	I		Float
$\overline{\text{EMS}}$	O	O		Float
$\overline{\text{EINT}}$	I	I		Float

Table 7-6. Pin Terminations (Cont'd)

Pin Name	I/O Tri-State (Z)	Reset State	Hi-Z* Caused By…	Unused Configuration
ECLK	I	I		Float
ELIN	I	I		Float
ELOUT	O	O		Float

NOTES
* Hi-Z = High impedance
1. CLKIN, RESET, and PF3:0/Mode D:Mode A are not included in the table because these pins must be used.
2. All bidirectional pins have tri-stated outputs. When a pin is configured as an output, the output is Hi-Z (high impedance) when inactive.

Recommendations for Unused Pins

The following is a list of recommendations for unused pins:

- If the CLKOUT pin is not used, turn it OFF, using CLKODIS in the SPORT0 Autobuffer Control register.
- If the Interrupt/Programmable Flag pins are not used, there are two options:
  - When these pins are configured as inputs at reset and function as interrupts and input flag pins, pull the pins High (inactive).
  - Program the unused pins as outputs. Set them to 1 prior to enabling interrupts and let the pins float.
- If a flag pin is not used, configure it as an output. If for some reason, you cannot configure it as an output, configure it as an input. Use a 100 kΩ pull-up resistor to V_{DD} (or, if this is not possible, use a 100 kΩ pull-down resistor to GND).

- If a SPORT is not used completely and if the SPORT pins do not have a second functionality, disable the SPORT and let the pins float.
- If the receiver on a SPORT is the only part being used, use resistors on the other pins. However, if the other pins are outputs, let them float.

Clock Signals

The ADSP-218x family processors may be operated with a TTL-compatible clock signal input to the CLKIN pin or with a crystal connected between the CLKIN and XTAL pins. If an external clock is used, XTAL must be left unconnected. The CLKIN signal may not be halted, changed, or operated below the specified frequency during normal operation.

The ADSP-218x family processors operate with an input clock frequency equal to half the instruction rate; for example, a 16.67 MHz input clock produces a 33 MHz instruction rate (30 ns cycle time). Device timing is relative to the internal clock rate which is indicated by the CLKOUT signal.

Because these processors include an on-chip oscillator circuit, an external crystal can be used. The crystal should be connected between the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 7-1. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used. The frequency value selected for the crystal should be half the desired instruction rate.

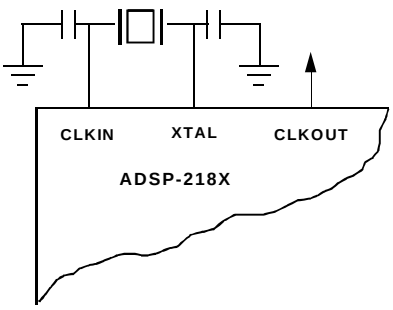

Figure 7-1. External Crystal Connections

Due to the high operating processor core clock speed requirements on some of the ADSP-218x DSPs, it may be advantageous to use a third-overtone crystal rather than a fundamental frequency crystal as an input clock signal in your design. Figure 7-2 shows a sample third overtone schematic.

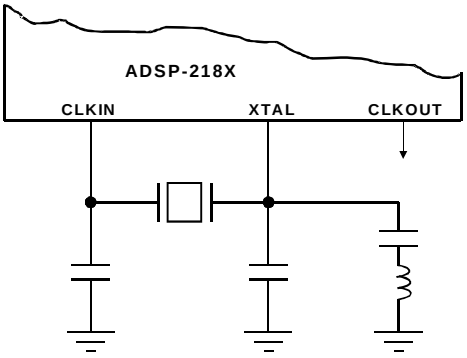

Figure 7-2. Third-Overtone Crystal

In this schematic, a parallel LC circuit is used as a bandpass filter to allow the third harmonic through to the crystal input of the DSP. For example, to operate an ADSP-2189M processor at 75 MHz, an input clock signal with a frequency of 37.5 MHz is required. Using a third overtone crystal circuit would allow you to use a 37.5 MHz third overtone crystal.

The internal phased lock loop (PLL) of the processors generates an internal clock that is four times the instruction rate.

The processors also generate a CLKOUT signal which is synchronized to the processors' internal cycles and operates at the instruction cycle rate. A phase-locked loop is used to generate CLKOUT and to divide each instruction cycle into a sequence of internal time periods called processor states. The relationship between the phases of CLKIN, CLKOUT, and the processor states is shown in Figure 7-3. The phases of the internal processor clock are dependent upon the period of the external clock.

The CLKOUT output can be disabled on the ADSP-218x processors. This is controlled by the CLKODIS bit in the SPORT0 Autobuffer Control Register.

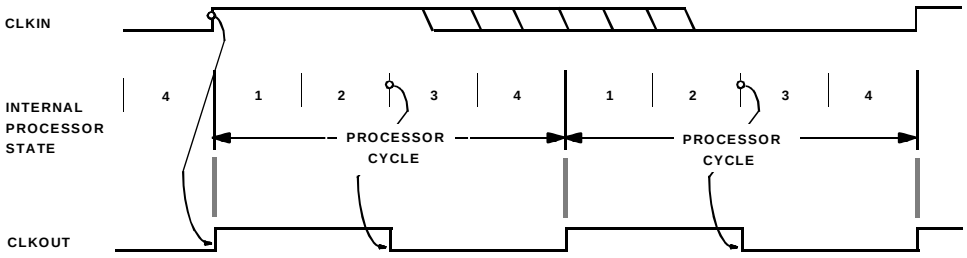

Figure 7-3. Clock Signals & Processor States

Synchronization Delay

Each processor has several asynchronous inputs (interrupt requests, for example), which can be asserted in arbitrary phase to the processor clock. The processor synchronizes such signals before recognizing them. The delay associated with signal recognition is called synchronization delay.

Different asynchronous inputs are recognized at different points in the processor cycle. Any asynchronous input must be valid prior to the recognition point to be recognized in a particular cycle. If an input does not meet the setup time on a given cycle, it is recognized either in the current cycle or during the next cycle if it remains valid.

Edge-sensitive interrupt requests are latched internally so that the request signal only has to meet the pulse width requirement. To ensure the recognition of any asynchronous input, however, the input must be asserted for at least one full processor cycle plus setup and hold time. Setup and hold times are specified in the data sheet for each individual device.

1/2x Clock Considerations

Each processor requires only a 1/2x frequency clock signal. They use what is effectively an on-chip phase-locked loop to generate the higher frequency internal clock signals and CLKOUT. Because these clocks are generated based on the rising edge of CLKIN, there is no ambiguity about the phase relationship of two processors sharing the same input clock. Multiple processor synchronization is simplified as a result.

Using a 1/2x frequency input clock with the phase-locked loop to generate the various internal clocks imposes certain restrictions. The CLKIN signal must be valid long enough to achieve phase lock before $\overline{\text{RESET}}$ can be deasserted. Also, the clock frequency cannot be changed unless the processor is in $\overline{\text{RESET}}$. Refer to the relevant ADSP-218x processor data sheet for details.

Resetting the Processor

The $\overline{\text{RESET}}$ signal halts execution and causes a hardware reset of the processor. The $\overline{\text{RESET}}$ signal must be asserted when the processor is powered up to assure proper initialization. $\overline{\text{RESET}}$ during initial powerup must be held long enough to allow the internal clock to stabilize.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid V_{DD} is applied to the processor and for the internal PLL to lock onto the specific crystal frequency. A minimum of 2000 CLKIN cycles ensures that the PLL has locked, but it does not include the crystal oscillator start-up time. During the power-up sequence the $\overline{\text{RESET}}$ signal should be held low.

If $\overline{\text{RESET}}$ is activated any time after powerup, the clock continues to run and does not require stabilization time.

If a clock has not been supplied during $\overline{\text{RESET}}$, the processor does not know it has been reset and the registers won't be initialized to the proper values.

At powerup, if $\overline{\text{RESET}}$ is held low (asserted) without any input clock signal, the states of the internal transistors are unknown and uncontrolled. This condition could lead to processor damage.

Table 7-8 on page 7-25 shows the $\overline{\text{RESET}}$ state of various registers, including the processors' on-chip memory-mapped status/control registers. The values of any registers not listed are undefined at reset. The contents of on-chip memory are unchanged after $\overline{\text{RESET}}$, except as shown in Table 7-8 on page 7-25 for the data-memory-mapped control/status registers. The CLKOUT signal continues to be generated by the processor during $\overline{\text{RESET}}$, except when disabled.

The contents of the computation unit (ALU, MAC, Shifter) and data address generator (DAG1, DAG2) registers are undefined following $\overline{\text{RESET}}$. When $\overline{\text{RESET}}$ is released, the processor's booting operation takes place, depending on the state of the processor's MMAP pin. (Program booting is described in Chapter 8, "Memory Interface".)

In a multiprocessing system with several processors, a synchronous $\overline{\text{RESET}}$ is required.

When the power supply and clock remain valid, the content of the on-chip memory is not changed by a pulsed $\overline{\text{RESET}}$ line.

Software-Forced Rebooting

Software-forced reboots can be accomplished in different ways. A software-forced reboot clears the context of the processor and initializes some registers. A *context clear* clears the processor stacks and restarts execution at address 0x0000. Table 7-7 shows the two different ways the ADSP-218x processor can perform a software reboot.

Table 7-7. Software-Forced Rebooting

Reboot Method	Description
Powerup Context Reset	Setting the PUCR bit in the SPORT1 Autobuffer and Powerdown Control register causes a reboot on recovery from powerdown
BDMA Context Reset	Setting the BCR bit in the BDMA Control register *before* writing to the BDMA Word Count register (BWCOUNT) causes a reboot. Execution starts after the BDMA reboot is completed.

Table 7-8 shows the state of the processor registers after a software-forced reboot. The values of any registers not listed are unchanged by a reboot.

During booting (and rebooting), all interrupts including serial port interrupts are masked and autobuffering is disabled. The serial port(s) remain active; one transfer—from internal shift register to data register—can occur for each serial port before there are overrun problems.

The timer runs during a reboot. If a timer interrupt occurs during the reboot, it is masked. Thus, if more than one timer interrupt occurs during the reboot, the processor latches only the first.

Table 7-8. ADSP-218x Processor State After Reset or Software Reboot

Control Field	Description	Reset	Reboot
Bus Exchange register			
PX	PX register	Undefined	Undefined
Status registers			
IMASK	Interrupt service enables	0	0
ASTAT	Arithmetic status	0	0
MSTAT	Mode status	0	Unchanged
SSTAT	Stack status	0x55	0x55
ICNTL	Interrupt control	Undefined	Unchanged
IFC	Interrupt force/clear	0	0

Table 7-8. ADSP-218x Processor State After Reset or Software Reboot (Cont'd)

Control Field	Description	Reset	Reboot
Control registers (memory-mapped)			
BPAGE	Boot page	0	Unchanged
SPORT1 configure	Configuration	1	Unchanged
SPE0	SPORT0 enable	0	Unchanged
SPE1	SPORT1 enable	0	Unchanged
TCOUNT	Timer count register	Undefined	Operates during reboot
TPERIOD	Timer period register	Undefined	Unchanged
TSCALE	Timer scale register	Undefined	Unchanged
PDFORCE	Powerdown force	0	Unchanged
PUCR	Powerup context reset	0	Unchanged
XTALDIS	XTAL pindrive disable during powerdown	0	Unchanged
XTALDELAY	Delay startup from power-down (4096 cycles)	0	Unchanged
Serial Port Control registers (memory-mapped, one set per SPORT)			
ISCLK	Internal serial clock	0	Unchanged
RFSR, TFSR	Frame sync required	0	Unchanged
RFSW, TFSW	Frame sync width	0	Unchanged
IRFS, ITFS	Internal frame sync	0	Unchanged

Table 7-8. ADSP-218x Processor State After Reset or Software Reboot (Cont'd)

Control Field	Description	Reset	Reboot
INVRFS, INVTFS	Invert frame sense	0	Unchanged
DTYPE	Companding type, format	0	Unchanged
SLEN	Serial word length	0	Unchanged
SCLKDIV	Serial clock divide	Undefined	Unchanged
RFSDIV	RFS divide	Undefined	Unchanged
Multichannel word enable bits		Undefined	Unchanged
MCE	Multichannel enable	0	Unchanged
MCL	Multichannel length	0	Unchanged
MFD	Multichannel frame delay	0	Unchanged
INVTDV	Invert transmit data valid	0	Unchanged
RBUF, TBUF	Autobuffering enable	0	0
TIREG, RIREG	Autobuffer I index	Undefined	Unchanged
TMREG, RMREG	Autobuffer M index	Undefined	Unchanged
FO *(SPORT1 only)*	Flag Out value	Undefined	Unchanged
CLKODIS	CLKOUT disable	0	Unchanged
BIASRND	MAC biased rounding	0	Unchanged

Table 7-8. ADSP-218x Processor State After Reset or Software Reboot (Cont'd)

Control Field	Description	Reset	Reboot
External Memory Control Registers (non-memory-mapped)			
DMOVLAY	Data memory overlay select	0	Unchanged
PMOVLAY	Program memory overlay select	0	Unchanged
External Memory Control registers (memory-mapped)			
DWAIT	Data memory overlay wait states	15 (M and N series DSPs only) 0x7 (All other DSPs)	Unchanged
PWAIT	Program memory overlay wait states	15 (M and N series DSPs only) 0x7 (All other DSPs)	Unchanged
BMWAIT	Byte memory wait states	15 (M and N series DSPs only) 0x7 (All other DSPs)	Unchanged
IOWAIT0-3	I/O memory wait states	15 (M and N series DSPs only) 0x7 (All other DSPs)	Unchanged
CMSSEL	Composite memory select	0xB	Unchanged

Table 7-8. ADSP-218x Processor State After Reset or Software Reboot (Cont'd)

Control Field	Description	Reset	Reboot
Programmable Flag Data & Control registers (memory-mapped)			
PFDATA	Programmable flag data	Undefined	Unchanged
PFTYPE	Programmable flag direction	0	Unchanged
DMA Control registers (memory-mapped)			
IDMAA	IDMA Internal Memory Address	Undefined	Unchanged
IDMAD	IDMA Destination Memory Type	Undefined	Unchanged
BIAD	BDMA Internal Memory Address	0	0x20[1]
BEAD	BDMA External Memory Address	0	0x60[1]
BTYPE	BDMA Transfer Word Type	0	Unchanged
BDIR	BDMA Transfer Direction	0	Unchanged
BCR	BDMA Context Reset	1	Unchanged
BWCOUNT	BDMA Word Count	0x20	0[1]
BMPAGE	External Byte Memory Page	0	0[1]

1 These values assume that you have just completed an initial BDMA boot load. For more information on BDMA register contents during the boot loading process see Table 7-9. These values will vary with a processor reboot (other than initial load), since they depend on the previous values.

Register Values for BDMA Booting

The state of some registers during reset and rebooting is influenced by the MMAP and BMODE pins in the ADSP-2181 and ADSP-2183 processors and in all other ADSP-218x processors when they are in Full Memory Mode. If these pins are set for a BDMA boot, the values in the BDMA registers change as shown in Table 7-9.

Table 7-9. BDMA Registers before and after Initial Boot Loading

Register	Description[1]	Value Before Boot	Value After Boot
BIAD	BDMA Internal Memory Address. Set for internal address 0.	0	0x20
BEAD	BDMA External Memory Address. Set for external address 0.	0	0x60
BTYPE	BDMA Transfer Word Type. Set for 24-bit program memory words.	0	0
BDIR	BDMA Transfer Direction. Set to transfer data from byte memory.	0	0
BMPAGE	BDMA Page Selection. Set to byte memory page 0.	0	0
BWCOUNT	BDMA Word Count. Set to transfer 32 words.	0x20	0
BMWAIT	BDMA Port Wait States. Set to 7 waits per transfer.	0xF (M and N series DSPs only) 0x7 (All other DSPs)	0xF (M and N series DSPs only) 0x7 (All other DSPs)

Table 7-9. BDMA Registers before and after Initial Boot Loading (Cont'd)

Register	Description[1]	Value Before Boot	Value After Boot
BCR	BDMA Context Reset[2]	1	1
BMOVLAY[3]	BDMA Overlay value	0	0

1 Assumes MMAP=0 and BMODE=0 for a BDMA boot (applies to ADSP-2181 and ADSP-2183 processors) or MODEA=0 and MODEB=0 for all other ADSP-218x processors).
2 Set to 1 to:
(a) Hold off instruction execution during BDMA transfer
(b) Start execution at address PM(0x0000) after BDMA transfer
(c) Leave a BDMA interrupt pending
This sequence of events occurs if BCR is set before BWCOUNT is written, or after the initial boot.
3 Applies only to the following processors: ADSP-2187L/N, ADSP-2188M/N, and ADSP-2189M/N.

External Interrupts

ADSP-218x family processors have a number of prioritized, individually maskable, external interrupts, which can be either level- or edge-triggered. These interrupt request pins are named $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$. The $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$ pins are only available as the (optional) alternate configuration of SPORT1. The configuration of SPORT1 as either a serial port or as interrupts (and flags) is determined by bit 10 of the processor's system control register.

The ADSP-218x processors also have two dedicated level-triggered interrupt request pins and one dedicated edge-triggered interrupt request pin; these are $\overline{\text{IRQL0}}$, $\overline{\text{IRQL1}}$, and $\overline{\text{IRQE}}$, respectively.

Internal interrupts, including serial port, timer, and DMA, are discussed in other chapters. Additional information about interrupt masking, set up, and operation can be found in Chapter 3, Program Sequencer.

Interrupt Sensitivity

Individual external interrupts can be configured in the ICNTL register as either level-sensitive or edge-sensitive.

Level-sensitive interrupts operate by asserting the interrupt request line ($\overline{\text{IRQx}}$) until the request is recognized by the processor. Once recognized, the request must be deasserted before unmasking the interrupt so that the DSP does not continually respond to the interrupt.

In contrast, edge-triggered interrupt requests are latched when any high-to-low transition occurs on the interrupt line. The processor latches the interrupt so that the request line may be held at any level for an arbitrarily long period between interrupts. This latch is automatically cleared when the interrupt is serviced. Edge-triggered interrupts require less external hardware than level-sensitive requests since there is never a need to hold or negate the request. With level-sensitive interrupts, however, many interrupting devices can share a single request input; this allows easy system expansion.

An interrupt request will be serviced if it is not masked (in the IMASK register) and a higher priority request is not pending. Valid requests initiate an interrupt servicing sequence that vectors the processor to the appropriate interrupt vector address. See Chapter 3, “Program Sequencer” for the ADSP-218x processor interrupt vector addresses. There is a synchronization delay associated with both external interrupt request lines and internal interrupts.

If an interrupt occurs during a waitstated external memory access or during the extra cycles required to execute an instruction that accesses external memory more than once, it is not recognized between the cycles, only before or after. Edge-sensitive interrupts are latched, but not serviced, during bus grant ($\overline{\text{BG}}$) unless the Go mode is enabled.

In order to service an interrupt, the processor must be running and executing instructions. The IDLE instruction can be used to effectively halt processor operations while waiting for an interrupt.

Edge-sensitive and level-sensitive interrupt requests are serviced similarly. Edge-sensitive interrupts may remain active (low) indefinitely, while level-sensitive interrupts must be deasserted before the RTI instruction is executed; otherwise, the same interrupt immediately recurs.

Care must be taken with the serial port (SPORT1) that can be configured for alternate functions ($\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$). If the RFS1 or TFS1 input is held low when SPORT1 is configured as the serial port and then is reconfigured as $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$, an interrupt request can be generated. This interrupt request can be cleared with the use of the IFC register.

Flag Pins

All ADSP-218x processors provide flag pins. The alternate configuration of SPORT1 includes a Flag In (FI) pin and a Flag Out (FO) pin. The configuration of SPORT1 as either a serial port or as flags and interrupts is selected by bit 10 of the processor's System Control register.

The FI pin can be used to control program branching, using the IF FLAG_IN and IF NOT FLAG_IN conditions of the JUMP and CALL instructions. These conditions are evaluated based on the last state of the FI pin; FLAG_IN is true if FI was last sampled as a 1 and false if last sampled as a 0. FO can be used as a general purpose external signal. The state of FO is also available as a read-only bit of the SPORT1 control register.

The ADSP-218x processors have three additional flag output pins: FL0, FL1, and FL2. These flags (and F0) can be controlled in software to signal events or conditions to any external device such as a host processor. The Modify Flag Out instruction, which is conditional, can perform SET, RESET and TOGGLE actions — this instruction allows programs executing on the DSP processor to control the state of its flag output pins. Note that if the condition in the Modify Flag Out instruction is CE (counter expired), the counter is not decremented as in other IF CE instructions.

Flag outputs FL0, FL1 and FL2 are set to 1 at $\overline{\text{RESET}}$. The Flag Out (F0) is not affected by $\overline{\text{RESET}}$.

The ADSP-218x processors have eight additional general-purpose flag pins, PF7-0. These flags can be programmed as either inputs or outputs; they default to inputs following reset. The PFx pins are programmed with the use of two memory-mapped registers. The Programmable Flag register (shown in Figure 7-4) determines the flag direction: 1=output and 0=input. The Programmable Flag Data register (shown in Figure 7-5) is used to read and write the values on the pins.

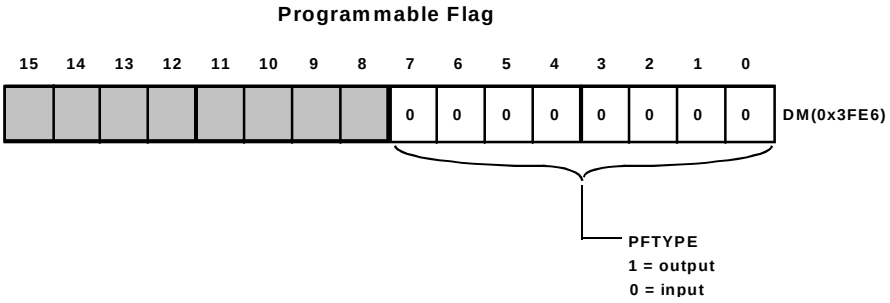

Figure 7-4. Programmable Flag Register

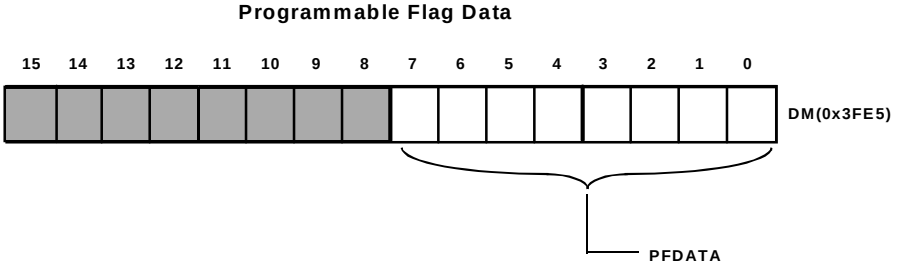

Figure 7-5. Programmable Flag Data Register

Data being read from a pin configured as an input is synchronized to the processor's clock. Pins configured as outputs drive the appropriate output value. When the PFDATA register is read, any pins configured as outputs will read back the value being driven out.

Powerup Issues

The ADSP-218x dual-voltage M and N series processors have special issues related to powerup. These issues include the powerup sequence and the dual-voltage power supplies. This section discusses both these issues. it also gives information about reset generators, which provide a reliable active reset once the power supplies and internal clock circuits have stabilized.

Powerup Sequence

The following recommendations should be observed when powering dual-voltage DSP's. Ideally the two supplies, V_{DDEXT} and V_{DDINT}, should be powered up together. If they cannot be powered up together, the internal (core) supply should be powered up first. Powering up the core supply first reduces the risk of latchup events.

A network of protection diodes, as shown in Figure 7-6, isolates the internal supplies and provides ESD protection for the IO pins. When applying power separately to the V_{DDINT} or V_{DDEXT} pins, care should be taken to limit the maximum supply current and duration that would be conducted through the isolation diodes if the unpowered pins are at ground potential.

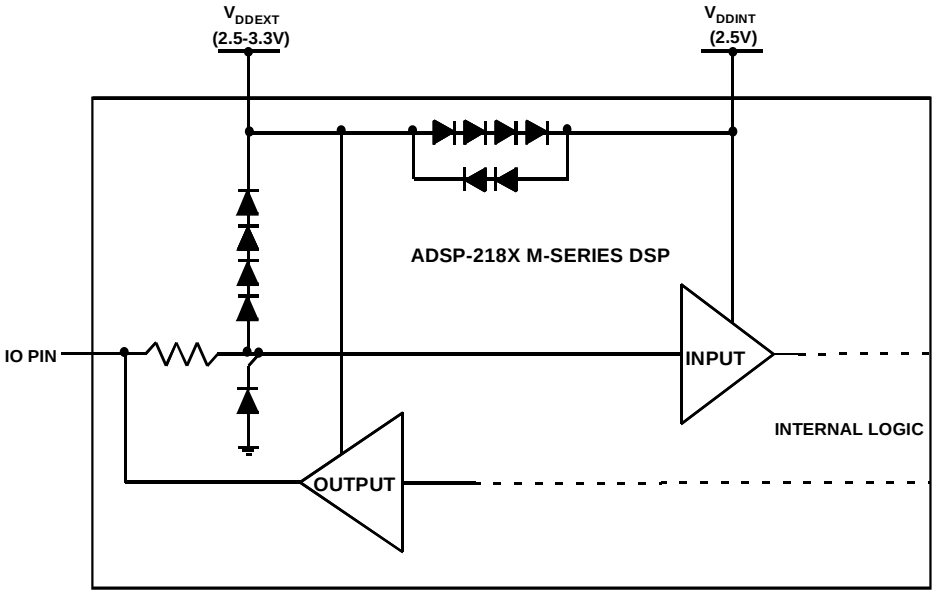

Figure 7-6. Protection Diodes and IO Pin ESD Protection

If an external master clock is used, it should not be driving the CLKIN pin when the DSP is unpowered. The clock must be driven immediately after powerup; otherwise, internal gates stay in an undefined (hot) state and can draw excess current. After powerup, there should be sufficient time for the internal PLL to stabilize (2000 clock cycles) before the reset is released.

In addition, time should be allowed for the oscillator to start up and reach full amplitude. This may take 100 ms, depending upon choice of crystal, operating frequency, loop gain, and capacitor ratios. Startup time may be more significant than the 2000 clock cycles needed for the PLL to stabilize.

Power Supplies

The following lists the power supplies that ADSP-218x processors can use:

- ADSP-218x L series processors use a single 3.3 V power supply
- ADSP-218x M series processors can use either a single 2.5 V power supply or a 2.5 V internal power supply and a 3.3 V power supply for I/O
- ADSP-218x N series processors can use either a single 1.8 V power supply or a 1.8 V internal power supply and either a 2.5 V or a 3.3 V power supply for I/O

Dual Supply Example

To provide 2.5 V and 3.3 V power supplies for the ADSP-218x M series processors, it is suggested that a dual regulator, powered from a common source, be used. Analog Devices does not currently have a 2.5 V/3.3 V dual-output regulator; however, it does have several suitable single output regulators.

We suggest the low drop-out regulators, ADP3330ART-2.5 and ADP3330ART-3.3, which are identical parts but with different (fixed) output voltages. These regulators are available in SOT-23-6, a very small, six lead surface mount package, and will provide 2.5 V @ 70 mA and 3.3 V @ 90 mA from a 5 V supply at ambient temperatures up to 85°C. This power supply is suitable for the dual-voltage M series of DSPs—up to their maximum operating temperature and clock frequencies.

These regulators also accept an active low, shut down signal, which is useful for many low power applications that require power saving schemes. An open collector output error signal is available to permit appropriate action in the event that the input voltage has fallen too low to permit efficient regulation.

Figure 7-6 provides a suggested schematic using these regulators.

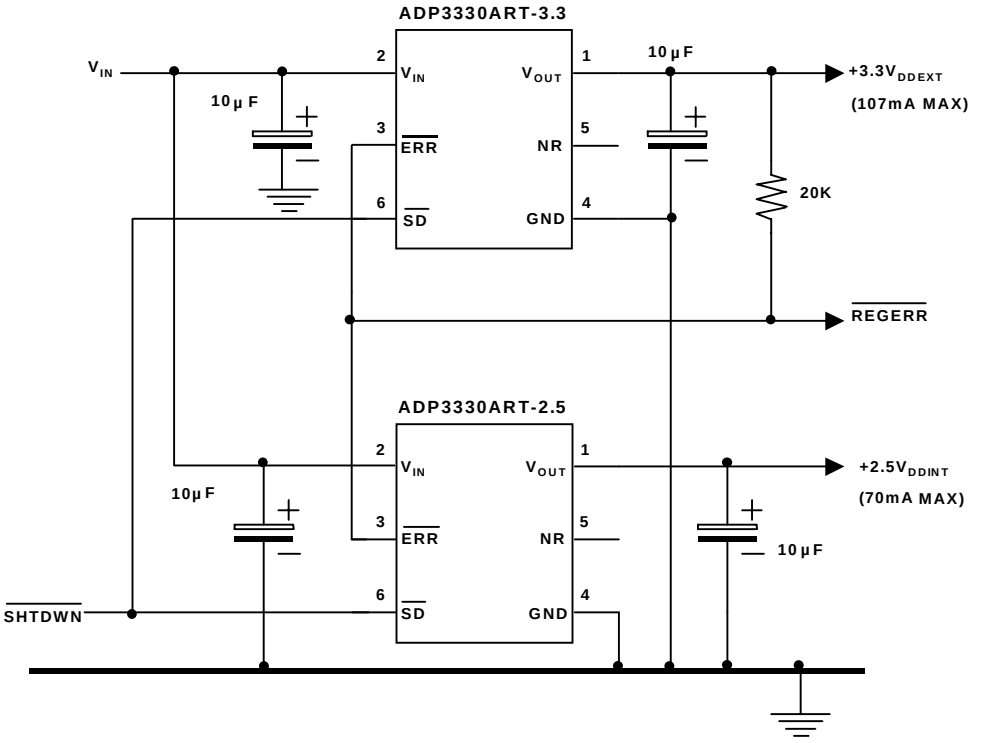

Figure 7-7. Suggested Dual Power Supply for ADSP-218x M Series DSPs

Reset Generators

It is important that a DSP (or programmable device) have a reliable active RESET that is released once the power supplies and internal clock circuits have stabilized. The RESET signal should not only offer a suitable delay, but it should also have a clean monotonic edge. Analog Devices has a range of microprocessor supervisory ICs with different features. Features include one or more of the following:

- Powerup reset
- Optional manual reset input
- Power low monitor
- Back-up battery switching

Part number series for Analog Devices' supervisory circuits are as follows:

- ADM69x
- ADM70x
- ADM80x
- ADM1232
- ADM181x
- ADM869x

A simple powerup reset circuit is shown below, using the ADM809-RART reset generator. The ADM809 provides an active low $\overline{\text{RESET}}$ signal whenever the supply voltage is below 2.63 V. At powerup, a 240 ms active reset delay is generated to give the power supplies and oscillators time to stabilize.

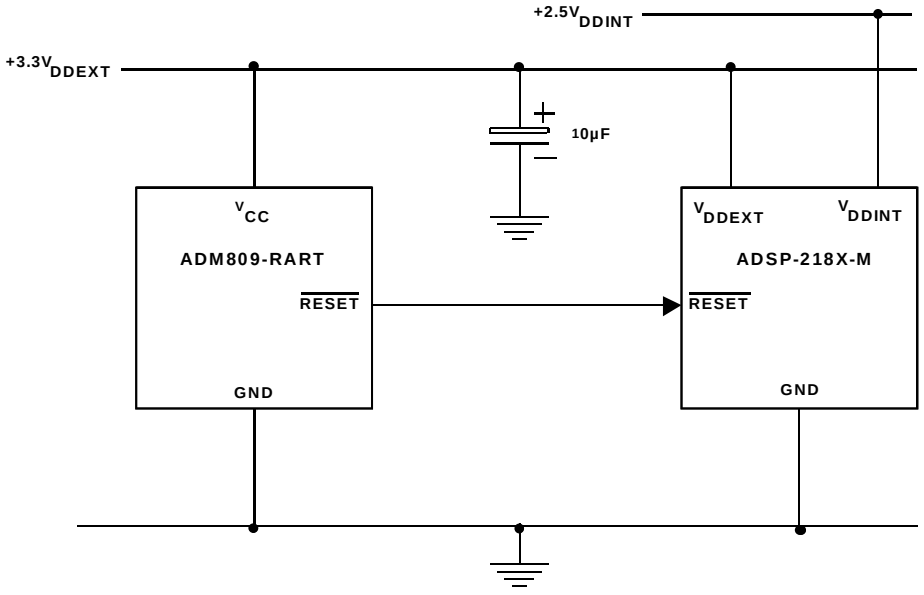

Figure 7-8. Simple Reset Generator for M Series DSPs

Another part, the ADM706TAR, provides poweron $\overline{\text{RESET}}$ and optional manual $\overline{\text{RESET}}$. It allows designers to create a more complete supervisory circuit that monitors the supply voltage. Monitoring the supply voltage allows the system to initiate an orderly shutdown in the event of power failure. The ADM706TAR also allows designers to create a watchdog timer that monitors for software failure. This part is available in an eight lead SOIC package. Figure 7-9 shows a typical application circuit using the ADM706TAR.

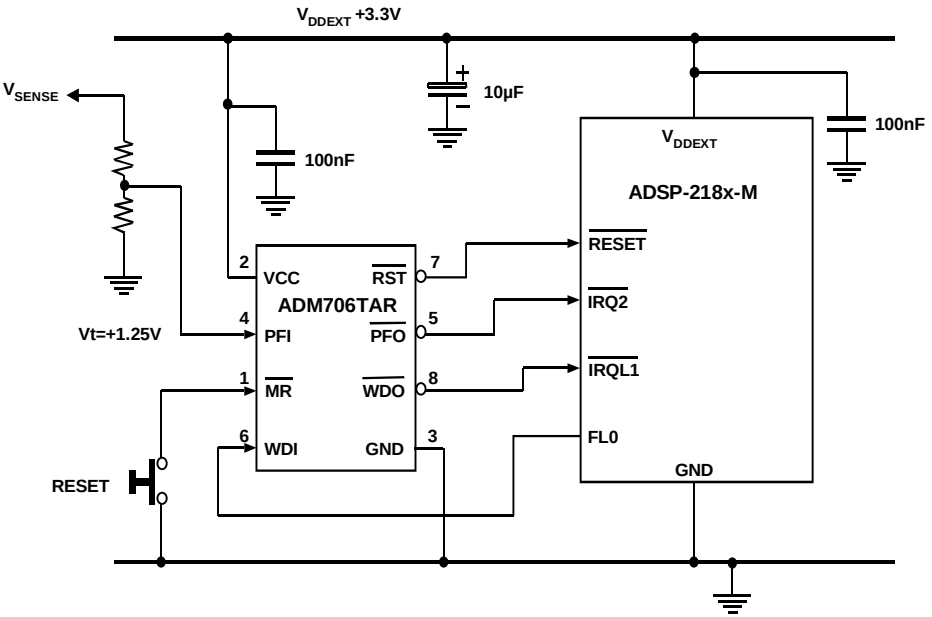

Figure 7-9. Reset Generator and Power Supply Monitor

Powerdown

The ADSP-218x processors provide a powerdown feature that allows the processor to enter a very low power dormant state through hardware or software control. In this CMOS standby state, power consumption is less than 1 mW (approximate). (Refer to the processor data sheet for exact power consumption specifications.)

The powerdown feature is useful for applications where power conservation is necessary, for example in battery-powered operation. Features of powerdown include:

- Internal clocks are disabled
- Processor registers and memory contents are maintained
- Ability to recover from powerdown in less than 100-400 CLKIN cycles (the number of cycles depends on the processor used in your system design; see the appropriate data sheet for information)
- Ability to disable internal oscillator when using crystal
- No need to shut down clock for lowest power when using external oscillator
- Interrupt support for executing “housekeeping” code before entering powerdown and after recovering from powerdown
- User selectable powerup context

Even though the processor is put into the powerdown mode, the lowest level of power consumption still might not be achieved if certain guidelines are not followed. Lowest possible power consumption requires no additional current flow through processor output pins and no switching activity on active input pins. Therefore, a careful analysis of pin loading in your circuit is required. The following sections detail the proper powerdown procedure as well as provide guidelines for clock and output pin connections required for optimum low-power performance.

Powerdown Control

You can control several parameters of powerdown operation through control bits in the SPORT1 Autobuffer/Powerdown Control Register.

This control register is memory-mapped at location 0x3FEF and is shown in Figure 7-10.

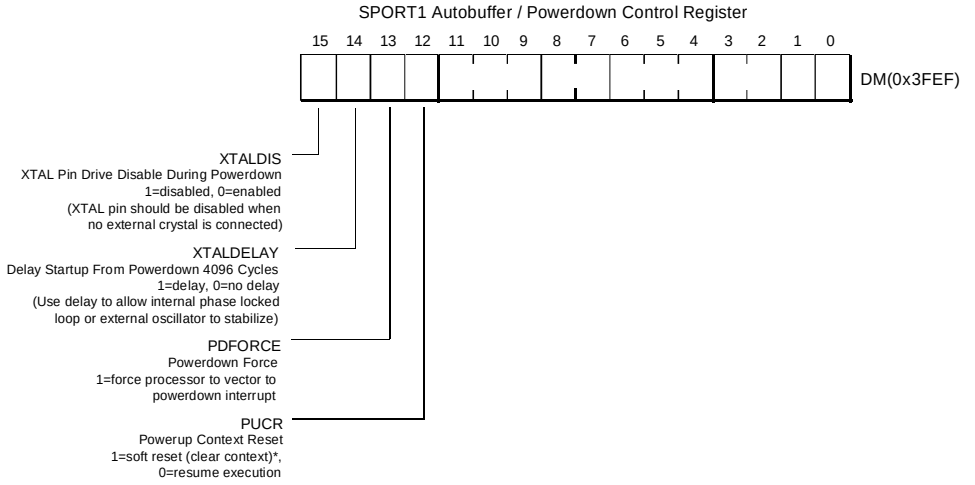

Figure 7-10. SPORT1 Autobuffer/Powerdown Control Register

Entering Powerdown

The powerdown sequence is defined as follows.

1. Initiate the powerdown sequence by applying a high-to-low transition to the $\overline{\text{PWD}}$ pin or by setting the powerdown force control bit (PDFORCE) in the SPORT1 Autobuffer/Powerdown Control Register (followed by a NOP instruction).

2. The processor vectors to the non-maskable powerdown interrupt vector at address 0x002C. (Note: The powerdown interrupt is never masked. You must be careful not to cause multiple powerdown interrupts to occur or stack overflow may result. Multiple powerdown interrupts can occur if the $\overline{\text{PWD}}$ input is pulsed while the processor is already servicing the powerdown interrupt.)

3. Any number of housekeeping instructions, starting at location 0x002C, can be executed prior to the processor entering the powerdown mode. Typically, this section of code is used to configure the powerdown state, disable on-chip peripherals and clear pending interrupts.

4. The processor now enters powerdown mode when it executes an IDLE instruction (while $\overline{\text{PWD}}$ is asserted). The processor may take either one or two cycles to power down depending upon internal clock states during the execution of the IDLE instruction. All register and memory contents are maintained while in powerdown. Also, all active outputs are held in whatever state they are in before going into powerdown.

If an RTI is executed before the IDLE instruction, then the processor returns from the powerdown interrupt and the powerdown sequence is aborted.

While the processor is in the powerdown mode, the processor is in CMOS standby. This allows the lowest level of power consumption where most input pins are ignored. Active inputs need to be held at CMOS levels to achieve lowest power. For more information, see “Processor Operation During Powerdown” on page 7-51.

Exiting Powerdown

The powerdown mode can be exited with the use of the $\overline{\text{PWD}}$ pin or with $\overline{\text{RESET}}$. There are also several user-selectable modes for start-up from powerdown which specify a start-up delay as well as specify the program flow after start-up. This allows the program to resume from where it left off before powerdown or for the program context to be cleared.

Ending Powerdown with the Powerdown Pin

Applying a low-to-high transition to the $\overline{\text{PWD}}$ pin will take the processor out of powerdown mode. You have the option of selecting the amount of time the processor takes to come out of the powerdown mode with the “delay start-up from powerdown” control bit (XTALDELAY), bit 14 in the Powerdown Control register. If this bit is cleared to 0, no additional delay is introduced over the quick start-up (between 100 and 400 cycles, as specified in the relevant ADSP-218x data sheet). If this bit is set to 1, a delay of 4096 cycles is introduced. The delay feature is used depending upon the state of an external clock oscillator at the time of powerup or if the internal clock is disabled. For more information, see the sections, “Systems Using an External TTL/CMOS Clock” on page 7-48 and “Systems Using a Crystal and the Internal Oscillator” on page 7-49.

You can also program one of two options directing the processor how to resume operation. The context for exiting powerdown is set by bit 12 (PUCR, powerup context reset) of the Powerdown Control register.

If the PUCR control bit is cleared to 0, the processor will continue to execute instructions following the IDLE instruction. For example, a high-to-low transition is applied to the pin, which causes the processor to vector to the powerdown interrupt routine. In this routine, a few housekeeping tasks are performed and the IDLE instruction is executed. The processor powers down. Some time later a low-to-high transition is applied to the pin, causing the processor to exit powerdown mode. Since the PUCR bit is 0, the processor resumes executing instructions in the powerdown interrupt routine, starting at the instruction following the IDLE instruction. When an RTI instruction is encountered, control then passes back to the main routine.

If the PUCR bit is set to 1 for a clear context, the processor resumes operation from powerdown by clearing the PC, STATUS, LOOP and CNTR stacks. The IMASK and ASTAT registers are set to 0 and the SSTAT goes to 0x55. The processor will start executing instructions from address 0x0000.

Ending Powerdown with the RESET Pin

If $\overline{\text{RESET}}$ is asserted while the processor is in the powerdown mode, the processor is reset and instructions are executed from address 0x0000. A boot is performed if the MMAP pin is set to 0 for the ADSP-2181 and ADSP-2183 processors or the MODE A and MODE B pins are set to 0 for all other ADSP-218x processors.

If the $\overline{\text{RESET}}$ pin is used to exit powerdown, then it must be held low for the appropriate number of cycles. If the clock is stopped at powerup or operating at a different frequency at powerup than it was before powerdown, $\overline{\text{RESET}}$ must be held long enough for the oscillator to stabilize plus an additional 1000 CLKIN cycles for the phase-locked loop to lock. The time required for the oscillator to stabilize depends upon the type of crystal used and capacitance of the external crystal circuit. Typically 2000 CLKIN cycles is adequate for clock stabilization time.

If the clock was not stopped at powerup and is at a stable frequency at powerup (same as before powerdown), only 5 cycles of $\overline{\text{RESET}}$ are required.

When ending powerdown with $\overline{\text{RESET}}$, the XTALDELAY (delay start-up from powerdown) control bit is ignored.

Startup Time after Powerdown

The time required to exit the powerdown state depends on whether an internal or external oscillator is used, and the method used to exit powerdown.

Systems Using an External TTL/CMOS Clock

When the processor is in powerdown, the external clock signal is ignored if the XTALDIS bit (XTAL pin disable) of the Powerdown Control register is set to 1. It is therefore not necessary to stop the external clock since no power is wasted while the external clock is running. If the external clock is to be stopped anyway, it must be kept running for (at least) one additional cycle after the IDLE instruction is executed.

The XTALDIS bit should always be set before entering powerdown. This specifies that the XTAL pin is not to be driven by the processor. During powerdown, there is no need to drive the XTAL pin when an external oscillator is used. Disabling the XTAL pin drive during powerdown lets the input clock run without wasting power.

After the processor is taken out of the powerdown mode by either the $\overline{\text{PWD}}$ pin or $\overline{\text{RESET}}$, it will begin executing instructions after a maximum start-up time of between 100 and 400 CLKIN cycles (see the relevant ADSP-218x data sheet for the correct specification) as long as the clock oscillator is stable and at the same frequency as before powerdown.

If the external clock is unstable when the processor exits powerdown, then the XTALDELAY control bit can be used. This allows time for the external clock to stabilize by inserting an additional 4096-cycle delay before the processor starts to execute instructions. The start-up delay can only be used when the processor is taken out of powerdown mode with the $\overline{\text{PWD}}$ pin.

If the processor is taken out of powerdown by $\overline{\text{RESET}}$ and the clock is stable and at the same frequency as before powerdown, $\overline{\text{RESET}}$ needs to be held for only 5 cycles.

Systems Using a Crystal and the Internal Oscillator

A trade-off can be made so that a fast start-up is possible, but power is consumed by leaving the oscillator running during powerdown. If a fast start-up is desired, then you must clear bits 14 (XTALDELAY) and 15 (XTALDIS) of the Powerdown Control Register to 0 before entering powerdown. This selects no additional delay after start-up from powerdown and drives the external crystal during powerdown. In this configuration, the oscillator will continue to operate and the processor will start executing instructions in less than 100 or 400 cycles after the low to high signal transition at the pin. (The number of cycles depends upon the processor used in your system design; please see the appropriate data sheet for specific timing information.) The XTAL pin will also be driven and the powerdown power consumption will be higher than the 1 mW specification. The following code example shows the powerdown interrupt routine.

```
/* Sample Powerdown Code */
/* Located at interrupt vector address 0x002C */
   pwd_int: ax0 = 0x0000; /* enable crystal, no delay */
      dm(0x3FEF) = ax0;
      idle;
      rti;
```

If the lowest possible power consumption is required, then you must set the XTALDELAY and XTALDIS bits to 1 before entering powerdown. This setting does the following:

- Selects the additional 4096 cycle delay to allow the oscillator to start and the phase locked loop to lock after start-up.
- Disables the drive to the XTAL pin during powerdown.

The following code example shows the powerdown interrupt routine.

```
/* Sample Powerdown Code */
/* Located at interrupt vector address 0x002C */
   pwd_int: ax0 = 0xC000; /* disable crystal, delay */
      dm(0x3FEF) = ax0;
      idle;
      rti;
```

Depending on the particular situation and external system conditions, the powerdown modes shown above could be set conditionally. If you want to powerdown for a long time you may want to set the mode for lowest power consumption. If you want to powerdown for a short time, lowest power consumption may not be that important.

If the $\overline{\text{RESET}}$ pin is used to exit powerdown and the clock has been stopped, then $\overline{\text{RESET}}$ must be held low for 1000 CLKIN cycles plus the time required for the phase locked loop to lock and the crystal oscillator to stabilize (typically 2000 CLKIN cycles.) If the clock is running during powerdown, a $\overline{\text{RESET}}$ signal of only 5 cycles is required.

Processor Operation During Powerdown

Some processor circuitry may still be active during powerdown mode. Also, some output pins remain active. A good understanding of these states will allow you to determine the best low-power configuration for your system. By keeping output loading and input switching to a minimum the lowest possible power consumption can be achieved.

Interrupts and Flags

Interrupts are latched and can be serviced if the processor exits powerdown without a context reset (PUCR=1). Any activity on the interrupt or flag input pins during powerdown will increase the power consumption. There should also be no resistive load on the flag output pins (as with any active output pin) if lowest power is desired.

SPORTs

The circuitry of the serial ports is not directly affected by powerdown. The SPORTs are indirectly affected if an internally generated SCLK or frame sync is required. SPORT circuitry continues to operate during powerdown.

It is possible to clock data into or out of the serial ports during powerdown. You must supply an external serial clock to support operation during powerdown. No interrupts or autobuffer operations will be serviced during powerdown. Instead, the SPORT interrupts are latched and can be serviced if the processor exits powerdown without resetting the processor. Data clocked into the processor will remain in the receive (RX) registers. Autobuffer transfers will occur after the device exits powerdown if the processor is not powered up with $\overline{\text{RESET}}$. Note that any SPORT activity will increase the power consumption above the 1 mW specification.

If an external serial clock and an external frame sync signal are supplied, data can be clocked into the RX register or out of the TX register during powerdown. Since the TX register can not be updated while the processor is in powerdown, the same value is repeatedly clocked out the serial port. Also, data in the RX register is continually overwritten since the RX register can not be read by the processor during powerdown.

If an external serial clock is used with an internal frame sync, frame sync signals continue to be generated during powerdown since they are derived from the serial clock. Data bits continue to be received with the RX register being overwritten. Since data is only transmitted when the TX register is written, data bits are only transferred out of the processor if the processor is put in powerdown during a serial port transfer. While the processor is being put into powerdown, the serial port transfer in progress is allowed to complete. Since an internally generated transmit frame sync is used, no subsequent frame syncs are generated while in powerdown.

If internal serial clock is used, there is no SPORT activity during powerdown; the serial clock stops.

Lowest power dissipation is achieved when active SPORT pins are not changing during powerdown and are held at CMOS levels.

IDMA Port During Powerdown

The IDMA port can receive data during powerdown, but it can not respond with an acknowledge ($\overline{\text{IACK}}$) signal or increment the IDMA internal address. If you are using a short read or short write and are in the middle of an IDMA transfer, you can complete a single read or write while the processor is in powerdown. If you are using the long read or long write method and are in the middle of an IDMA transfer, your host must be able to handle a "timeout" condition, as the DSP will not return an acknowledge to the transfer in process.

Note that IDMA activity while the DSP is in powerdown uses power and should be avoided to conserve power. For more information on lowest power use, see For more information, see "Conditions for Lowest Power Consumption" on page 7-54.

BDMA Port During Powerdown

Do not powerdown the ADSP-218x processor during a BDMA transfer. If you do, the DSP will not be able to recover correctly from powerdown and the contents of memory accessed by the processor's BDMA port will be corrupted.

If you need to go into powerdown mode, either:

- Verify that the BWCOUNT register contains a zero. If a BDMA transfer is in process, poll the BWCOUNT register to determine when the transfer is done.

  or

- Abort any BDMA transfer in progress by writing 1 to the BWCOUNT register and go into powerdown when the BWCOUNT register contains a zero. (Note that the BDMA transfer is not properly completed in this case.)

Conditions for Lowest Power Consumption

The state of all processor pins during powerdown is shown in Table 7-10.

To assure the lowest power consumption, all active input pins should be held at a CMOS level (to ground level, if possible). All active output pins should be free of resistive load since load current will increase power dissipation. You must perform a careful analysis of each input and output pin in order to insure lowest power dissipation.

Some inputs are active but ignored. The state of these inputs does not matter as long as they are at a CMOS level.

Table 7-10. Pin States During Powerdown

Pin	Direction	State During Powerdown
$\overline{\text{RESET}}$	I	Active
$\overline{\text{PWD}}$	I	Active
$\overline{\text{IRQ2}}$	I	Active, latched but not serviced
$\overline{\text{IRQE}}$	I	Active, latched but not serviced
$\overline{\text{IRQL0}}$	I	Active, latched but not serviced
$\overline{\text{IRQL1}}$	I	Active, latched but not serviced
MMAP	I	Active
$\overline{\text{BR}}$	I	Active, no response until after powerdown
$\overline{\text{BG}}$	O	Driven HIGH unless bus is granted
CLKIN	I	Input buffer inactive, but XTAL oscillator is active unless XTALDIS bit is set
CLKOUT	O	Driven HIGH

Table 7-10. Pin States During Powerdown (Cont'd)

Pin	Direction	State During Powerdown
XTAL	O	Driven HIGH if XTALDIS set, inversion of CLKIN otherwise
PWDACK	O	Driven HIGH
$\overline{\text{PMS}}$	O	Driven HIGH, high impedance if bus granted
$\overline{\text{DMS}}$	O	Driven HIGH, high impedance if bus granted
$\overline{\text{BMS}}$	O	Driven HIGH, high impedance if bus granted
$\overline{\text{IOMS}}$	O	Driven HIGH, high impedance if bus granted
$\overline{\text{CMS}}$	O	Driven HIGH, high impedance if bus granted
$\overline{\text{RD}}$	O	Driven HIGH, high impedance if bus granted
$\overline{\text{WR}}$	O	Driven HIGH, high impedance if bus granted
ADDR<13:0>	O	High impedance
DATA<23:0>	I	Inactive
DATA<23:0>	O	High impedance
SCLK0	I	Active
SCLK0	O	Driven to static level if internal, high impedance otherwise
TFS0	I	Active if SPORT 0 is enabled
TFS0	O	Driven if configured internal or in multichannel mode and SPORT 0 enabled, high impedance otherwise
RFS0	I	Active if SPORT 0 is enabled

Table 7-10. Pin States During Powerdown (Cont'd)

Pin	Direction	State During Powerdown
RFS0	O	Driven if configured internal and SPORT 0 enabled, high impedance otherwise
DR0	I	Active if SPORT 0 is enabled
DT0	O	Driven if serial port operating. Output may be static or changing depending upon serial clock, high impedance otherwise
SCLK1	I	Active
SCLK1	O	Driven to a static level if internal, high impedance otherwise
TFS1/$\overline{\text{IRQ1}}$	I	Active if SPORT 1 is enabled or configured alternate ($\overline{\text{IRQ1}}$)
TFS1	O	Driven if SPORT 1 is enabled and configured for internal transmit framing, high impedance otherwise
RFS1/$\overline{\text{IRQ0}}$	I	Active if SPORT 1 is enabled or configured alternate ($\overline{\text{IRQ0}}$)
RFS1	O	Driven if SPORT 1 is enabled and configured for internal receive framing, high impedance otherwise
DR1/FI	I	Active if SPORT 1 is enabled or configured alternate (FI)
DT1/FO	O	Driven if serial port operating. Output may be static or changing depending upon serial clock. Driven if SPORT 1 is enabled or configured alternate (FO)
FL<2:0>	O	Driven to previous value

Table 7-10. Pin States During Powerdown (Cont'd)

Pin	Direction	State During Powerdown
PF<7:0>	I/O	Active
BMODE	I	Active
$\overline{\text{IRD}}$	I	Active, if $\overline{\text{IS}}$ asserted
$\overline{\text{IWR}}$	I	Active, if $\overline{\text{IS}}$ asserted
$\overline{\text{IS}}$	I	Active
IAL	I	Active, if $\overline{\text{IS}}$ asserted
IAD	I/O	Active, if an operation in progress
$\overline{\text{IACK}}$	O	Active

PWDACK Pin

The powerdown acknowledge pin (PWDACK) is an output that indicates when the processor is powered down. This pin is driven high by the processor when it has powered down and is driven low when the processor has completed its powerup sequence. A low level on the PWDACK pin also indicates that there is a valid CLKOUT signal and that instruction execution has begun. Figure 7-11 shows an example of timing for the powerdown and restart sequence.

The processor is executing code when the $\overline{\text{PWD}}$ pin is brought low. The processor vectors to the powerdown interrupt vector and an IDLE instruction is executed causing the processor to go into powerdown. The CLKOUT and PWDACK signals are driven high by the processor. At this point, the input clock pin is ignored. If the processor is put into the powerdown mode via the powerdown force bit in the powerdown control register, the result is the same as described above.

The input clock is started and the $\overline{\text{PWD}}$ pin is brought high. After the necessary start-up cycles the processor brings the PWDACK output low, begins driving the CLKOUT pin with a clock signal and begins to fetch the instruction after the IDLE instruction. The processor then resumes normal operation.

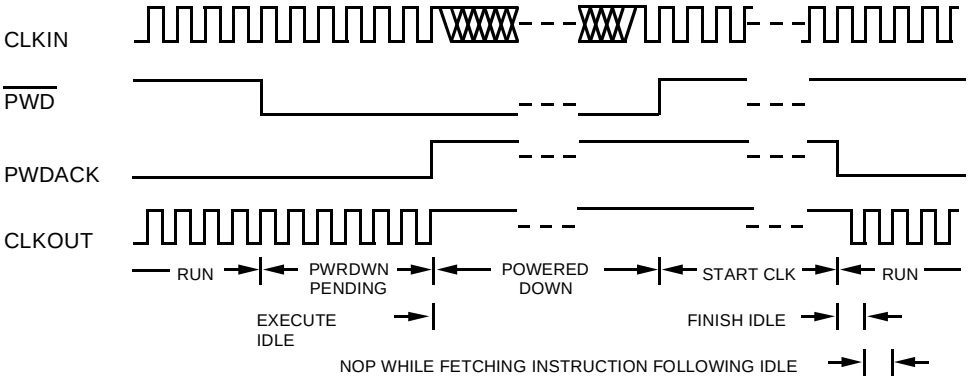

Figure 7-11. Powerdown Timing Examples

When powerdown is terminated with the $\overline{\text{RESET}}$ pin or if a start-up delay is selected, a low level on the PWDACK pin only indicates the start of oscillations on the CLKOUT pin. It will not necessarily indicate the start of instruction execution.

The state of PWDACK and also the CLKOUT signal is undefined during the first 100 cycles of initial reset.

Using Powerdown as a Non-Maskable Interrupt

The powerdown interrupt is never masked. It is possible to use this interrupt for other purposes if desired. The processor will not go into powerdown until an IDLE instruction is executed. If an RTI is executed before the IDLE instruction, then the processor returns from the powerdown interrupt and the powerdown sequence is aborted.

It is possible to place a series of instructions at the powerdown interrupt vector location 0x002C. This routine should end with an RTI instruction and not contain an IDLE instruction if the interrupt is to be used for purposes other than powerdown.

Bus Request/Grant

This section describes the bus request and grant feature of the ADSP-218x processors.

An ADSP-218x processors can relinquish control of data and address buses to an external device. The external device requests the bus by asserting (low) the bus request signal, $\overline{\text{BR}}$. The $\overline{\text{BR}}$ signal is an asynchronous input. If the ADSP-218x processor is not performing an external access, it responds to the active $\overline{\text{BR}}$ input in the following processor cycle by:

1. Tristating the data and address buses and the $\overline{\text{xMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$ output drivers,
2. Asserting the bus grant ($\overline{\text{BG}}$) signal, and
3. Halting program execution (unless Go mode is enabled).

If Go mode is enabled, the ADSP-218x processor continues to execute instructions from its internal memory. It will not halt program execution until it encounters an instruction that requires an external access. (An external access may be either a memory device access or a memory overlay access, BDMA access, or I/O space access.)

If Go mode is not enabled, the ADSP-218x processor always halts before granting the bus. The processor's internal state is not affected by granting the bus, and the serial ports remain active during a bus grant, whether or not the processor core halts.

If the ADSP-218x processor is performing an external access when the $\overline{BR}$ signal is asserted, it will not grant the buses until the cycle after the access completes. The sequence of events is illustrated in Figure 7-12. The entire instruction does not need to be completed when the bus is granted. If a single instruction requires two external accesses, the bus will be granted between the two accesses. The second access is performed after $\overline{BR}$ is removed.

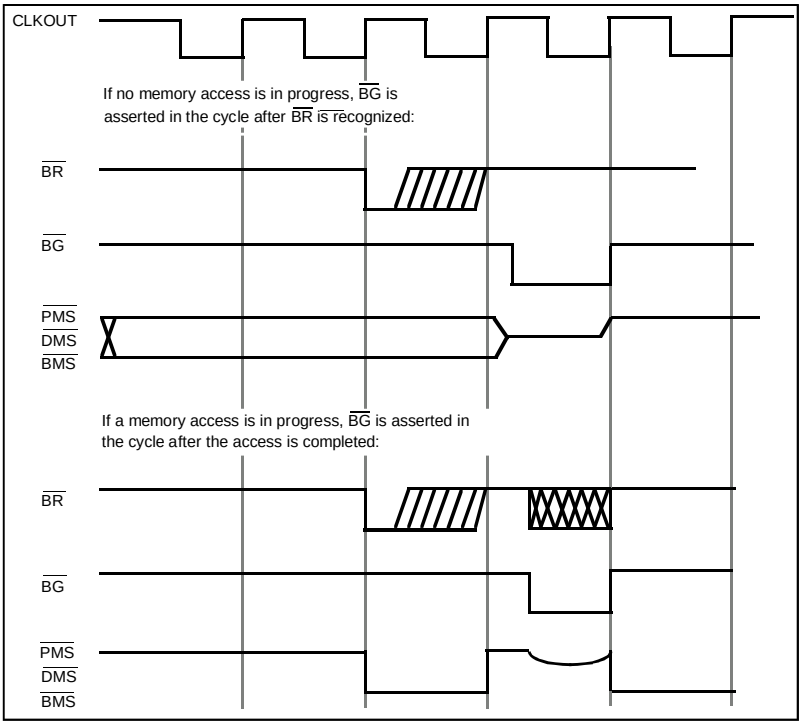

Figure 7-12. Bus Request (With or Without External Access)

When the $\overline{BR}$ input is released, the ADSP-218x processor releases the $\overline{BG}$ signal, reenables the output drivers and continues program execution from the point where it stopped. $\overline{BG}$ is always deasserted in the same cycle that the removal of $\overline{BR}$ is recognized. Refer to the data sheet for exact timing relationships.

The bus request feature operates at all times, including when the processor is booting and when $\overline{RESET}$ is active. During $\overline{RESET}$, $\overline{BG}$ is asserted in the same cycle that $\overline{BR}$ is recognized. During booting, the bus is granted after completion of loading of the current byte (including any wait states). Using bus request during booting is one way to bring the booting operation under control of a host computer.

The ADSP-218x processors also have a Bus Grant Hung ($\overline{BGH}$) output, which lets them operate in a multiprocessor system with a minimum number of wasted cycles. The $\overline{BGH}$ pin asserts when the ADSP-218x processor is ready to execute an instruction but is stopped because the external bus is granted to another device. The other device can release the bus by deasserting bus request. Once the bus is released, the ADSP-218x processor deasserts $\overline{BG}$ and $\overline{BGH}$ and executes the external access.

Target System Hardware

This section provides target system hardware recommendations to assist you in preventing problems with an EZ-ICE emulation system.

Target Board Connector for EZ-ICE Probe

The ADSP-218x processor has on-chip emulation support and an ICE-port, which is comprised of a special set of pins that interface to the EZ-ICE. By using only a 14-pin connection from the target system to the EZ-ICE, this interface allows for in-circuit emulation without replacing the target system processor. This 14-pin connection is a standard, 0.100-inch on-center, pin-strip header. Target systems must have a 14-pin connector to accept the EZ-ICE's in-circuit probe, a 14-pin female plug.

Figure 7-13 shows the EZ-ICE connector (a standard pin strip header). You must add this connector to your target board design if you intend to use the EZ-ICE.

Be sure to allow enough room in your system to fit the EZ-ICE probe onto the 14-pin connector.

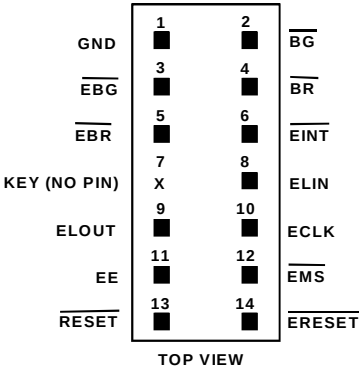

Figure 7-13. EZ-ICE Connector

The 14-pin, 2-row pin strip header is keyed at the Pin 7 location—you must remove Pin 7 from the header. The pins must be 0.025 inches square and at least 0.20 inches in length. Pin spacing should be 0.1 x 0.1 inches. The pin strip header must have at least a 0.15 inch clearance on all sides to accept the EZ-ICE probe plug.

Pin strip headers are available from vendors such as 3M, McKenzie (Framatome Connectors International), and Samtec, Inc.

The ICE-Port interface consists of the following ADSP-218x processor pins: $\overline{\text{EBR}}$, $\overline{\text{EINT}}$, EE, $\overline{\text{EBG}}$, ECLK, $\overline{\text{ERESET}}$, ELIN, $\overline{\text{EMS}}$, and ELOUT. These ADSP-218x processor pins must be connected only to the EZ-ICE connector in the target system. These pins have no function, other than during emulation, and do not require pull-up or pull-down resistors. All of the emulator signals become active once the Emulation Enable (EE) signal is driven high.

The traces for these signals between the ADSP-218x processor and the connector must be kept as short as possible — no longer than 3 inches.

The following pins are also used by the EZ-ICE: $\overline{\text{BR}}$, $\overline{\text{BG}}$, $\overline{\text{RESET}}$, and GND.

The EZ-ICE uses the EE signal to take control of the ADSP-218x processor in the target system. This causes the processor to use its $\overline{\text{ERESET}}$, $\overline{\text{EBR}}$, and $\overline{\text{EBG}}$ pins instead of the $\overline{\text{RESET}}$, $\overline{\text{BR}}$, and $\overline{\text{BG}}$ pins. The $\overline{\text{BG}}$ output is tri-stated.

These signals do not need to be jumper-isolated in your system.

The EZ-ICE connects to your target system via a ribbon cable and a 14-pin female plug. The female plug is plugged onto the 14-pin connector (a pin strip header) on the target board.

Using Mode Pins with RESET and ERESET Signals

Issuing the CHIP RESET command during emulation causes the DSP to perform a full chip reset. The state of the Mode pins are latched upon the rising edge of the $\overline{\text{RESET}}$ signal; this holds true when the DSP is reset in a running system or when a CHIP RESET command is issued when in emulation mode.

Therefore, when using the EZ-ICE with a 100-pin ADSP-218x processor, it is vital that the Mode pins are set correctly *prior to* issuing a CHIP RESET command from the emulator user interface.

If you are using a passive method of maintaining mode information (as discussed in "Active or Passive Mode Pin Configuration" on page 7-13), then it does not matter that the mode information is latched by an emulator reset. However, if you are using the RESET pin as a method of actively setting the value of the Mode pins, then you need to take into consideration the effects of an emulator reset.

One method of ensuring that the values located on the Mode pins are those desired is to construct a circuit like the one shown in Figure 7-14. The circuit shown in this figure forces the value located on the Mode A pin to a logic high, regardless of whether it is latched via the $\overline{\text{RESET}}$ or $\overline{\text{ERESET}}$ pin. (To configure the Mode pin to a logic low, you could use a two-input AND gate with the $\overline{\text{ERESET}}$ and $\overline{\text{RESET}}$ signals connected as inputs and the output of the AND gate connected to the Mode pin. In this example, the Mode pin would be driven to a logic low when either the $\overline{\text{RESET}}$ or the $\overline{\text{ERESET}}$ signals go active low.)

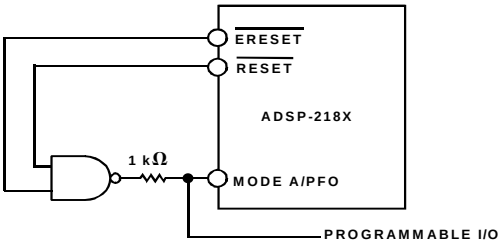

Figure 7-14. EZ-ICE Circuit for ADSP218x Mode Pins

Bus Request Signal

The Bus Request signal ($\overline{\text{BR}}$) should be pulled high with a 10 kΩ resistor if it is not being used in your system design. Failure to pull $\overline{\text{BR}}$ high may result in the inability of EZ-ICE to fully initialize when connected to a target. Since the microcontroller uses the Bus Request signal to communicate with the DSP, it is critical that you do not leave $\overline{\text{BR}}$ floating, even if you are not using it in your target.

When not using the emulator, the $\overline{BR}$ pin must be pulled high. If it is not pulled high, either a hold-off condition could occur, which can halt the DSP from booting either via BDMA or IDMA, or program execution could halt indefinitely. Typical behavior for this problem would be no activity on the $\overline{BMS}$ signal, or the $\overline{IACK}$ signal staying inactive (high) indefinitely.

Memory Select Signals

All memory select signals should be pulled high for EZ-ICE emulator compatibility.

You must connect a pull-up resistor (10 kΩ) on the memory select signals ($\overline{RD}$, $\overline{WR}$, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$, and $\overline{IOMS}$) if they are used in your target system. (For example, you would use these signals when accessing external memory or memory-mapped peripheral devices.) Pull-up resistors are needed since there are no internal pull-ups to guarantee the memory select signal's state during prolonged tri-stated conditions, which result from typical EZ-ICE debugging sessions. Because the EZ-ICE uses the DSP's bus to communicate with Program Memory (PM), Data Memory (DM), Boot Memory (BM), Input Output Memory (IOM), and Emulator Memory Space, pull-up resistors must be used.

Decoupling Capacitors

0.1 µF decoupling capacitors should be placed (as close to the DSP as possible) on all V_{DD} pins connected to the same digital ground.

During clock and data transitions, when all signal pins switch simultaneously, decoupling capacitors provide a localized source DC voltage and current for optimal operation of the DSP. Decoupling capacitors also ensures that there is a low-impedance power source present in power planes and circuit traces. They effectively remove high frequencies from the signal trace while not affecting lower frequencies.

All other digital integrated circuit chips in your system should be decoupled to manufacturers recommendations.

Also, a 100 µF bypass capacitor can be placed at the rails of the power supply coming into the target board to filter unwanted RF noise from the power supply cable.

RESET Signal

Due to the high operating speeds of RC circuits, using them to delay the deassertion of the $\overline{\text{RESET}}$ signal at powerup is not recommended for ADSP-218x processor systems. During powerup, $\overline{\text{RESET}}$ must be held low for a minimum of 2000 DSP CLKIN cycles to ensure proper phase-lock loop of the internal processor clock. Achieving proper phase-lock loop ensures that the CLKOUT signal phase-locks with the CLKIN signal.

A Schmitt Trigger (or some type of hysteresis circuitry) should be used on the reset line to minimize "ringing" on the $\overline{\text{RESET}}$ signal or to allow for mechanical debouncing of a push button or switch. A clean $\overline{\text{RESET}}$ signal that is free from ringing or glitches guarantees proper DSP powerup and initialization. Without a Schmitt Trigger, the $\overline{\text{RESET}}$ signal may oscillate or ring before settling to a valid inactive (high) level. Ringing on the $\overline{\text{RESET}}$ signal may cause the DSP to lock up, since the $\overline{\text{RESET}}$ signal may fall below the V_{IH} minimum voltage specification. When the signal falls below this minimum, a faulty reset that does not meet the 2000 CLKIN cycle minimum DSP specification can occur.

PCB Board

Whenever possible, target systems should consist of a multilayered PCB board with a separate power and ground plane stacked in the middle layers of the board. Wirewrapped boards are not generally recommended as they are more susceptible to external noise and parasitic capacitance.

EZ-ICE Powerup Procedure

The ADSP-218x EZ-ICE communicates with a host PC over an RS232 serial cable. Connect the ADSP-218x EZ-ICE board to the selected COM port of the PC (COM1 or COM2) using the attached RS232 serial cable of the emulator.

Below is the recommended powerup sequence when using the emulator to debug your target system:

1. Power up the ADSP-218x EZ-ICE by using the supplied power adapter. Also, power up your target system.
2. Using the provided ground cable, attach one end of the ground cable to the emulator probe at reference location TP1. Attach the other end of the ground cable to a proper ground on your target system.
3. Attach the emulator probe to your target board's 14-pin emulator header.
4. Invoke the emulator software.

Reverse this procedure for removing the ADSP-218x EZ-Ice from your target system.

Other Considerations

When designing a target system, keep the following in mind:

- EZ-ICE emulation introduces an up to 15 pF load on the $\overline{\text{RESET}}$ and $\overline{\text{BR}}$ signals. See the *ADSP-218x Family Hardware Installation Guide* for more details.
- EZ-ICE emulation introduces an up to 15 pF load on the $\overline{\text{BG}}$ signal. In some modes the EZ-ICE drives the $\overline{\text{BG}}$ signal. See the *ADSP-218x Family Hardware Installation Guide* for more details.

- EZ-ICE emulation ignores $\overline{\text{RESET}}$ and $\overline{\text{BR}}$ when single-stepping.
- EZ-ICE emulation ignores $\overline{\text{RESET}}$ and $\overline{\text{BR}}$ when in Emulator Space (DSP Halted).
- EZ-ICE emulation ignores the state of the target $\overline{\text{BR}}$ in certain modes. As a result, the target system may take control of the DSP's external memory bus only if bus grant ($\overline{\text{BG}}$) is asserted by the EZ-ICE board's DSP.
- EZ-ICE emulation introduces a 500 µs latency between transitions to User Space and some signal responses. This latency occurs when you start (or resume) running your DSP program. The latency is the time between resumption of code execution and the EZ-ICE board allowing the DSP to respond to $\overline{\text{RESET}}$ and $\overline{\text{BR}}$.

Recommended Reading

The text *High-Speed Digital Design: A Handbook of Black Magic* is recommended for further reading. This book is a technical reference that covers the problems encountered in state-of-the-art, high-frequency digital circuit design, and is an excellent source of information and practical ideas. Topics covered in the book include:

- High-Speed Properties of Logic Gates
- Measurement Techniques
- Transmission Lines
- Ground Planes & Layer Stacking
- Terminations
- Vias
- Power Systems

- Connectors
- Ribbon Cables
- Clock Distribution
- Clock Oscillators

Reference: Johnson & Graham, *High-Speed Digital Design: A Handbook of Black Magic*, Prentice Hall, Inc., ISBN 0-13-395724-1.