Designing Boards with Atmel AT89C51, AT89C52, AT89C1051, and AT89C2051 for Writing Flash at In-Circuit Test

Recent improvements in chips and testers have made it possible for the tester to begin taking over the role traditionally assigned to the PROM programmer. Instead of having a PROM programmer write nonvolatile memories before assembling the board, the in-circuit tester writes them during in-circuit testing operations. Many Teradyne Z18-series testers are now in use loading code into nonvolatile memories, microcontrollers and in-circuit programmable logic devices. The purpose of this note is to explain how the Z18 approaches the writing task for Atmel AT89C series IC's, so that designers of boards using these chips can get the best results.

To write the flash memories embedded in the Atmel AT89C series chips, the Z18-family tester must be equipped with the Digital Function Processor (DFP) option.

The Atmel Technical Brief titled "Integrated Flash Memory Gives AT89C51 In-System Reprogrammability" describes two approaches, one parallel and the other serial. The Teradyne Z18XX tester with DFP can work with either, but this paper will only discuss the parallel approach. The serial method looks simpler at first glance, but you must consider that the AT89C series which serves as the serial interface must also have its code loaded by the tester. At some point, therefore, the parallel method must be used.

The Parallel Approach

There are some simple, yet important, design constraints for the parallel approach, as pointed out in the Atmel Technical Brief. If these constraints have not been observed during board design, it may not be possible for a tester to write the chip's flash memory, and the chip will have to be written with a PROM programmer before being installed on the board. There are four main ways to interfere with the tester's attempts to write the flash memory. The four Don'ts:

- Don't tie needed input pins to V_{CC} or ground;
- Don't tie needed input pins to outputs of other IC's;
- Don't tie supervoltage input pins to components that won't tolerate the voltage;
- Don't tie output pins needed for checking the write operation to other IC outputs.

It is always possible to design a board within the constraints described here. The Atmel Technical Brief points out specific pins that need attention, and explains how to work with these pins to insure in-circuit writability. These are discussed in detail below.

$\overline{EA}/V_{PP}$ (AT89C51/52) or RST/V_{PP} (AT89C1051/2051)

The tester will take this pin high during flash memory write and erase operations. $\overline{EA}/V_{PP}$ (AT89C51/52) or RST/V_{PP} (AT89C1051/2051) will generally be fixed either high or low when the board is carrying out its normal mission, depending on whether the application uses external addressing or runs entirely on its internal memory. There are four things to remember about this pin.

1. In certain parts of the Atmel documentation, Atmel recommends

Designing Boards with Atmel Flash Microcontrollers

Application Note

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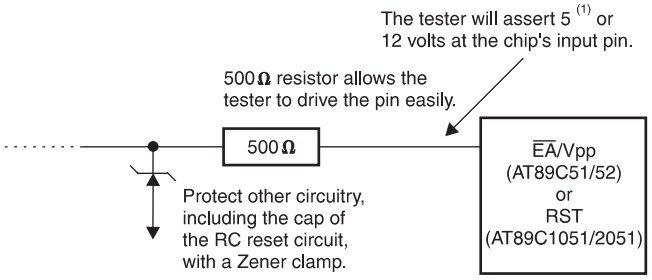
that this pin be "strapped" to V_{CC} or ground. Please interpret the word "Strapped" to mean "connected by a 500 Ω resistor." The resistor will supply the desired 0 or 1 logic level during normal board operation, but the tester can also change the level easily as needed when testing the microcontroller or when writing its flash memory.

2. The pin must be accessible to the tester, i.e. it must be contactable by a probe in a vacuum fixture (bed-of-nails fixture).
3. Atmel makes two versions of the microcontroller. One writes flash memory with 5 volts on this pin; the other writes flash memory with 12 volts on this pin. If you are using the 12-volt part, and if you need to connect other components to the $\overline{EA}/V_{PP}$ pin for any reason, you will need to provide some way of protecting the other components from being damaged by the 12-volt level. The AT89C1051/2051 are only available with 12-volt programming.
4. For the AT89C1051/2051, if an RC circuit is used to generate power-up reset, don't tie the capacitor directly to the RST pin. Put a resistor in between so that the tester will not have to take time charging the capacitor to 12 volts with each programmed byte.

Figure 1. Allow the tester to control $\overline{EA}/V_{PP}$/RST, and protect surrounding devices.



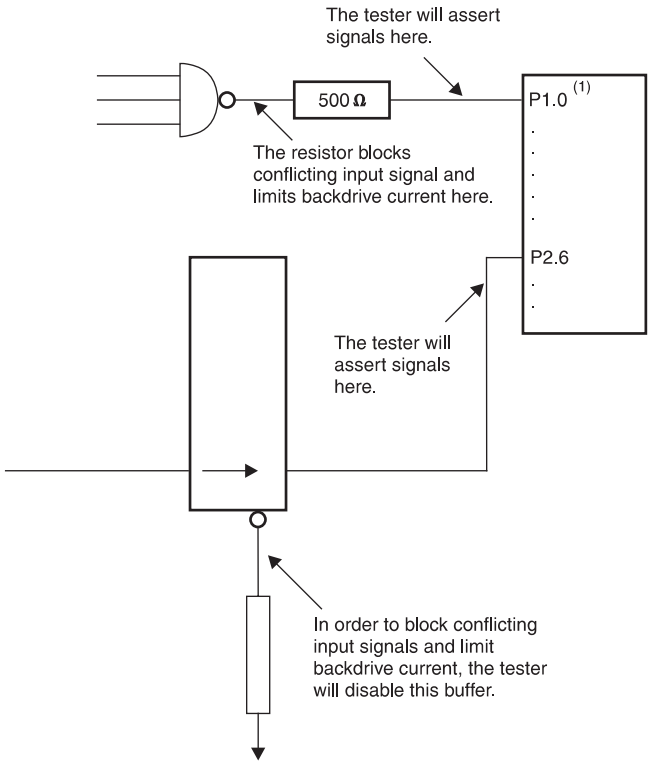
Note: 1. Only for the AT89C51 or AT89C52

Data Ports (P0, P1, P2, P3 for AT89C51/52 and P1, P3 for AT89C1051/2051)

The normal mission of the board may set these ports up to be outputs, or inputs, or a mix of outputs and inputs. During flash memory write and erase operations, the tester will apply signals to some of these pins, and attempt to read signals from others. Outputs of other circuits on the board may be exposed to excessive backdrive, or may interfere with output signals trying to come from the microcontroller. There are three things to remember about these pins.

1. The pins must be accessible to the tester, i.e. it must be contactable by probes in a vacuum fixture.
2. If any other chips have their outputs connected to pins used as inputs, they must be protected from backdrive signals coming from the tester. Pass such signals through disableable buffers as shown in Figure 2 below. Alternatively you may insert a 500 Ω resistor in series with such an output as also shown in Figure 2 below. The resistor will limit the backdrive current to 5 volts/500 ohms = 10 milliamps. The port pins used as inputs are all of P0, all of P1, P2.0-P2.4, P2.6, P2.7, P3.6, and P3.7 for the AT89C51/52 and P1 for the AT89C1051/2051.

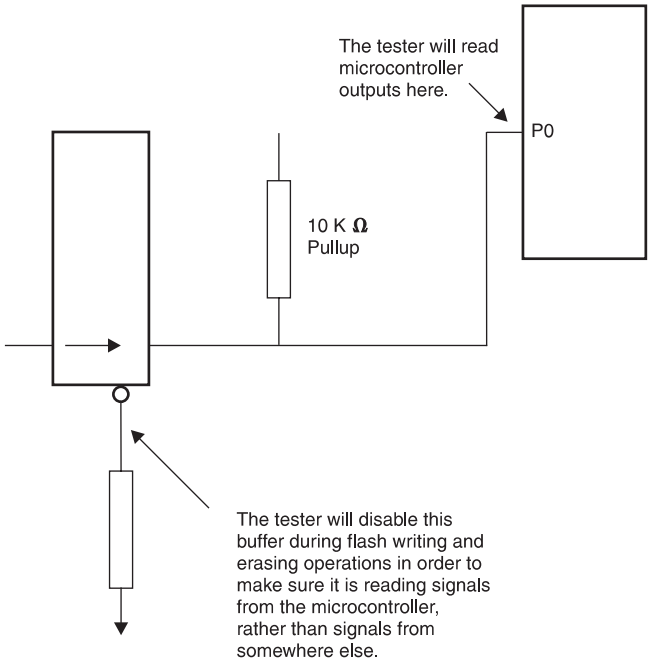
Figure 2. Allow the tester to assert signals safely on microcontroller pins that serve as inputs during flash memory writing and erasing.



Note: 1. For the AT89C1051/2051 the tester disable P1 input signals originating on the board during flash memory writing and erasing.

3. If any other chips have their outputs connected to pins used as outputs during flash memory writing and erasing operations, pass such signals through disableable buffers as shown in Figure 3. Attempting to isolate with a 500 Ω resistor will not work, due to the small amount of output current available from the device. A 10K pullup is required to ensure an adequate high for the tester to measure. The port pins used as inputs are all of P0 and P3.4 for the AT89C51/52 and P1 for the AT89C1051/2051.

Figure 3. Be sure spurious signals do not conflict with AT89C51/52 pins used as outputs during flash writing and erasing.



Note on Lock Bits

Do not program the DFP to set any of the Lock Bits until you are certain the other parts of the flash writing program have been fully debugged.

DFP Wiring

One possible way of wiring the DFP to write the devices is described in the tables. Two DR2p cards (that is, one from the base unit and one expansion kit) are required for one AT89C51/52 chip, and one DR2p card is required for each AT89C1051/2051 chip on the board.

Using the Atmel AT89C51 or AT89C52

RST

The tester will take this pin high during flash memory write and erase operations. It will be low when the board is carrying out its normal mission, unless frequent resetting is an integral part of the board's normal mission. There are three things to remember about this pin.

1. Most AT89C52 circuits have a simple RC reset circuit in which a large capacitor is wired between the RST pin and ground. When the tester drives the RST pin high to initiate an erasure or writing of the flash memory, several microseconds may be required to allow the tester's channel driver to charge the capacitor.
2. The pin must be accessible to the tester, i.e. it must be contactable by probe in a vacuum fixture.
3. Because the tester will force the pin high, you must design other circuitry on this pin to permit and tolerate the forced high.

PSEN

The tester takes this pin low during flash memory write and erase operations. Other than that, it is not supposed to be connected to anything else. There is one thing to remember about this pin.

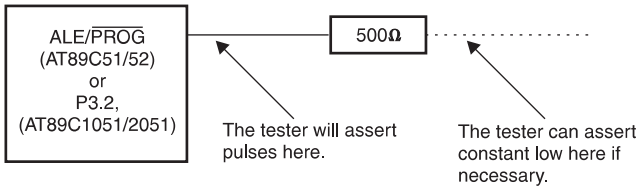
1. The pin must be accessible to the tester, i.e. it must be contactable by probe in a vacuum fixture.

ALE/$\overline{\text{PROG}}$

This pin is normally an output from the chip, but the tester will use it as a command strobe input during flash memory write and erase operations. There are three things to remember about this pin.

1. The pin must be accessible to the tester, i.e. it must be contactable by a probe in a vacuum fixture.
2. If any other chips have their outputs connected to this pin (unlikely, but please check) they must be capable of being disabled by the tester. Alternatively you may design a 500 Ω resistor in series with such an output. The resistor will protect the other chip from excessive backdrive, and will also prevent the other chip from volunteering spurious strobes during the flash memory writing or erasing processes.

Figure 4. 500 Ω resistor allows the tester to drive the ALE/$\overline{\text{PROG}}$ for AT89C51/52 or P3.2 (AT89C1051/2051) pin easily and keeps downstream circuits from seeing unusual activity.



3. Flash memory writing and erasing cycles generate activity in other parts of the circuit. If any other chips or subsystems on the board are designed to respond to the ALE signal, they will receive unusual instructions during the writing and erasing cycles. Be sure that this unusual activity does not damage them. Things to look for are other in-circuit writable nonvolatile devices, fusible squibs, etc. If any such exist, the 500 Ω resistor method described above for disabling outputs will also the tester to prevent the sensitive subsystems from seeing the unusual ALE activity.

AT89C51/52 Pin Name	DR2p Signal Name/Node#	Notes
P0.0	192 (DR2p 0 - group A)	Portwise Bidirectional
P0.1	193 (DR2p 0 - group A)	
P0.2	194 (DR2p 0 - group A)	
P0.3	195 (DR2p 0 - group A)	
P0.4	196 (DR2p 0 - group A)	
P0.5	197 (DR2p 0 - group A)	
P0.6	198 (DR2p 0 - group A)	
P0.7	199 (DR2p 0 - group A)	
P1.0 (A0)	224 (DR2p 1 - group A and B)	Address counter - 13 bits
P1.1 (A1)	225 (DR2p 1 - group A and B)	
P1.2 (A2)	226 (DR2p 1 - group A and B)	
P1.3 (A3)	227 (DR2p 1 - group A and B)	
P1.4 (A4)	228 (DR2p 1 - group A and B)	
P1.5 (A5)	229 (DR2p 1 - group A and B)	
P1.6 (A6)	230 (DR2p 1 - group A and B)	
P1.7 (A7)	231 (DR2p 1 - group A and B)	
P2.0 (A8)	232 (DR2p 1 - group A and B)	
P2.1 (A9)	233 (DR2p 1 - group A and B)	
P2.2 (A10)	234 (DR2p 1 - group A and B)	
P2.3 (A11)	235 (DR2p 1 - group A and B)	
P2.4 (A12)	236 (DR2p 1 - group A and B)	
P2.6	200 (DR2p 0 - group B)	Outputs from DFP to DUT
P2.7	201 (DR2p 0 - group B)	
P3.6	202 (DR2p 0 - group B)	
P3.7	203 (DR2p 0 - group B)	
RST	204 (DR2p 0 - group B)	
$\overline{EA}/V_{PP}$	205 (DR2p 0 - group B)	
ALE/$\overline{PROG}$	206 (DR2p 0 - group B)	
$\overline{PSEN}$	207 (DR2p 0 - group B)	
P3.4 (RDY/$\overline{BUSY}$)	208 (DR2p 0 - group C)	Input from DFP to DUT

Clock

The AT89C51/52 Clock must be running during flash writing. Most boards have clock circuits which will be normally running while the board is on its fixture with power applied. If the program contains a feature that disables the clock, you will need to defeat it for the duration of this test page. If you use a single-chip fixture to debug your application, you will need to add a crystal in the single-chip fixture.

Using the Atmel AT89C1051 or AT89C2051

XTAL1

The tester will apply logic level signals to this pin during flash memory write and erase operations. There are two things to remember about this pin.

1. The pin must be accessible to the tester, i.e. it must be contactable by probe in a vacuum fixture.
2. Because the tester will force high and low signals on this pin, you must design other circuitry on this pin to permit and tolerate the logic level signals applied by the tester.

P3 Pins P3.2 .. P3.5 and P3.7

The tester applies logic level signals to these five pins during flash memory write and erase operations. There are three things to remember about this group of pins.

1. The pins must be accessible to the tester, i.e. they must be contactable by probes in a bed-of-nails fixture.
2. If your application uses these pins as inputs, and any other chips have their outputs connected to these pins, the other chips' outputs must be capable of being disabled by the tester, or in any case must tolerate the logic level high and low signals applied by the tester. Alternatively you may design a 500 Ω resistor in series with the other chip's outputs. The resistor will protect the other chip from excessive backdrive, and will also prevent the other chip from interfering with the tester's signals during the flash memory writing or erasing processes. Pay special attention to intermittent signal sources such as interrupts or external or external timing inputs that are usually connected to P3.2, P3.3, P3.4.
3. Flash memory writing and erasing cycles generate activity in other parts of the circuit. If any other chips or subsystems on the board are designed to respond to the P3 signals, they will receive unusual instructions during the writing and erasing cycles. Be sure that this unusual activity does not damage them. Things to look for are other in-circuit writable nonvolatile devices, high current drivers, fusible squibs, etc. If any such exist, the 500 Ω resistor method described for RST will also allow the tester to prevent the sensitive subsystems from seeing the unusual signal activity. Because the flash writing signals are logic level, not 12-volt, the zener diodes noted for RST are not necessary on the P3 signals. See Figure 4.

Note on V_{PP}

Generation of V_{PP} by the DFP on channel 223 presents no danger to the conventional digital driver and receiver on channel 223, because the conventional driver and receiver are disconnected by a D relay during DFP operations. In your DFP program, make sure to set V_{PP} to zero and disconnect the V_{PP} relay before exiting from ptprog.c.

AT89C1051/205252 Pin Name	DR2p Signal Name/Node#	Notes
P1.0	192 (DR2p 0 - group A)	Portwise Bidirectional
P1.1	193 (DR2p 0 - group A)	
P1.2	194 (DR2p 0 - group A)	
P1.3	195 (DR2p 0 - group A)	
P1.4	196 (DR2p 0 - group A)	
P1.5	197 (DR2p 0 - group A)	
P1.6	198 (DR2p 0 - group A)	
P1.7	199 (DR2p 0 - group A)	
P3.2/$\overline{\text{PROG}}$	200 (DR2p 0 - group B)	Outputs from DFP to DUT
P3.3	201 (DR2p 0 - group B)	
P3.4	202 (DR2p 0 - group B)	
P3.5	203 (DR2p 0 - group B)	
P3.7	204 (DR2p 0 - group B)	
RST/V_{PP}	223 (DR2p 0 - group D)	V_{PP} supplied by DFP